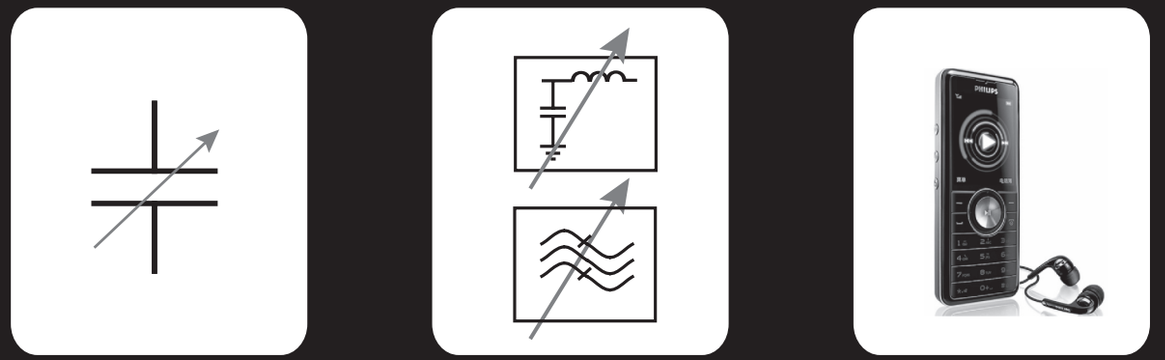
Thin Film Barium Strontium Titanate Capacitors for Tunable RF Front-end Applications

M.P.J. Tiggelman

ISBN 978-90-365-2937-2

Thin Film Barium Strontium Titanate Capacitors for Tunable RF Front-end Applications



M.P.J. Tiggelman

THIN FILM BARIUM STRONTIUM TITANATE CAPACITORS FOR TUNABLE RF FRONT-END APPLICATIONS

Markus Petrus Josephus Tiggelman

Samenstelling promotiecommissie:

Voorzitter:	prof.dr.ir. A.J. Mouthaan	Universiteit Twente
Secretaris:	prof.dr.ir. A.J. Mouthaan	Universiteit Twente
Promotor:	prof.dr. J. Schmitz	Universiteit Twente
Ass. Promotor:	dr.ir. R.J.E. Hueting	Universiteit Twente
Referent:	dr. K. Reimann	NXP Semiconductors
Leden:	prof.dr.ing. D.H.A. Blank	Universiteit Twente
	prof.dr.ir. B. Nauta	Universiteit Twente
	prof.dr.ir. R.A.M. Wolters	Universiteit Twente, NXP Semiconductors
	adj.prof.dr.ir. R. Jos	Universiteit Chalmers, NXP Semiconductors

Ph.D. dissertation:	University of Twente, The Netherlands.
Title:	THIN FILM BARIUM STRONTIUM TITANATE CAPACITORS FOR TUNABLE RF FRONT-END APPLICATIONS
Author:	M.P.J. Tiggelman
ISBN:	978-90-365-2937-2
Printing:	Printservice Technical University of Eindhoven.

This research was funded by NXP Semiconductors in cooperation with Philips Research Laboratories and the University of Twente. Partial support came from the European IST project NANOSTAR.

THIN FILM BARIUM STRONTIUM TITANATE CAPACITORS FOR TUNABLE RF FRONT-END APPLICATIONS

PROEFSCHRIFT

ter verkrijging van
de graad van doctor aan de Universiteit Twente,
op gezag van de rector magnificus,
prof.dr. H. Brinksma,
volgens besluit van het College voor Promoties
in het openbaar te verdedigen
op donderdag 3 december 2009 om 16:45 uur

door

Markus Petrus Josephus Tiggelman
geboren op 4 oktober 1977
te Enschede

Dit proefschrift is goedgekeurd door:

de promotor:	prof.dr. J. Schmitz
de ass. promotor:	dr.ir. R.J.E. Hueting

Contents

Chapter 1

Introduction

Mobile phone technology, and more in general wireless technology, demands every year, cheaper and more compact electronic circuitry with more extended functionality. By developing innovative electronic components and by designing state of the art system solutions this request can be fulfilled.
In this dissertation we discuss a component for wireless communication, which is used to electrically tune the radio frequency. The tuning of the resonance frequency can be compared by mechanically turning the knob of a classic radio to tune in on a different radio channel.

The radio spectrum, including radio frequencies (RF), covers the frequencies between 3 MHz–30 GHz [1]. An RF signal is an alternating electrical signal, which can propagate through dielectrics like air and SiO_2. Applications like, a mobile phone transmits and receives RF signals containing speech or text data.
A mobile phone nowadays can operate at 4 dissimilar (quad-band) radio frequency bands around 850 MHz, 900 MHz, 1800 MHz, and 1900 MHz [2]. The band of operation depends in which part of the world the user operates his or her cellphone.

One of the most important hardware parts in a mobile phone is the RF front-end [3], which consists of a number of electronic circuits.
A *single-band* RF front-end exists of at least a power amplifier (PA), a low-noise amplifier (LNA), a transmit and a receive (duplex) filter, an antenna, and an impedance matching network [3]. The PA amplifies the outgoing signal up to a few watts of power in mobile phones. The LNA amplifies the

incoming signal for further processing.
A duplex bandpass filter contains a receive and a transmit band. This bandpass filter strongly suppresses out-of-band signals and only in a limited frequency band a signal can be either transmitted or received, without too much attenuation. The antenna receives and transmits the RF signals.
The purpose of an impedance matching network is to have an optimal power flow from the source to the load to avoid reflections. Preferably the load of the impedance matching network has to absorb all of the power transmitted from the source. To achieve this the source impedance should be equal to the load impedance. A single band RF front-end is realized without any tunable components.

As stated before, modern versatile cellular phones support a large number of standards and frequency bands [2]. For *multi-band* operation multiple non-tunable circuits can be selected by employing multiple switches. Some of these fixed circuits can be replaced by a single tunable circuit to save precious space and components on a printed circuit board.
Reconfigurable circuits can tune in on multiple frequencies and can support different standards. A simplified example is given for a dual-band cellphone containing a bandpass filter building block in an RF front-end (see Figure 1.1). A dualband cellphone has two bandpass receive filters, which are set to two different receive frequency bands. Likewise for the transmit bandpass filters. The architecture can consist of 4 separate non-tunable bandpass filter circuits, or 1 tunable bandpass filter which is able to tune in the receive or transmit frequency band of interest, as depicted in Figure 1.1. Tunable components can decrease the dimensions of electronic circuits by exploiting the circuits' reconfigurability.

Most passive tunable technologies are still in the research and development phase and are being optimized for radio frequency (RF) architectures, especially focused on the RF front-end (see Figure 1.2).

The PA and LNA of a multi-band tunable RF front-end both contain active non-tunable components. The three remaining building blocks can be designed with solely passive (tunable) components.
The impedance of the antenna is susceptible to environmental changes in the band of operation [4], e.g., bringing a cellphone to your ear changes the reactive part of the antenna impedance. If the antenna impedance is not corrected for the new load impedance, then the PA will deliver a higher

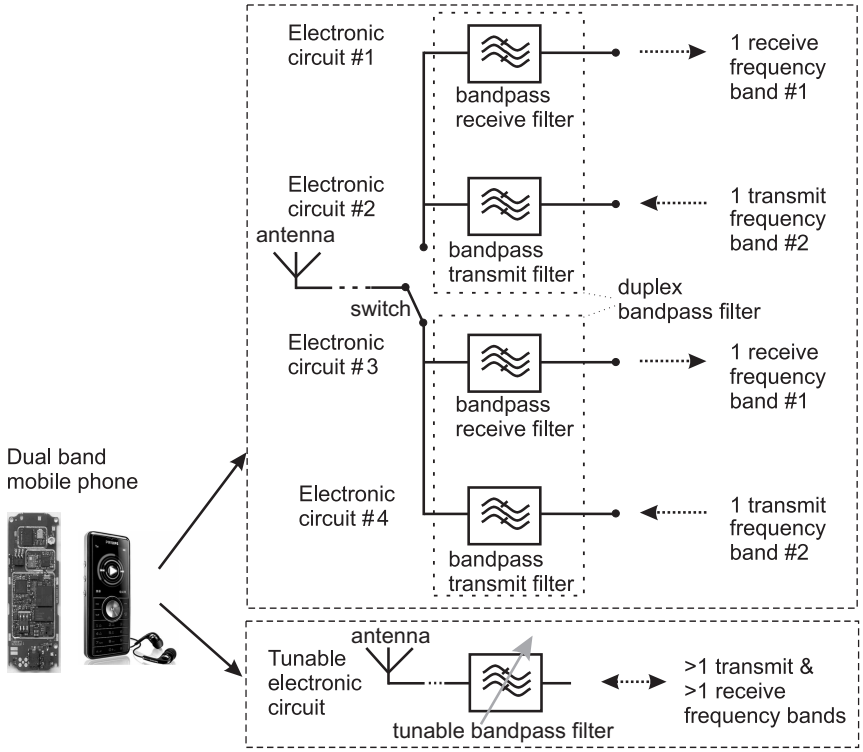


Figure 1.1 – A simplified example of two design options for a dual-band transmit and receive filter in a mobile phone that supports 4 frequency bands: 1) a design containing 4 separate electronic circuits which support each a single frequency band in which the phone can either receive or transmit signals, or 2) a design containing a single electronic tunable circuit, which supports 4 or more frequency bands.

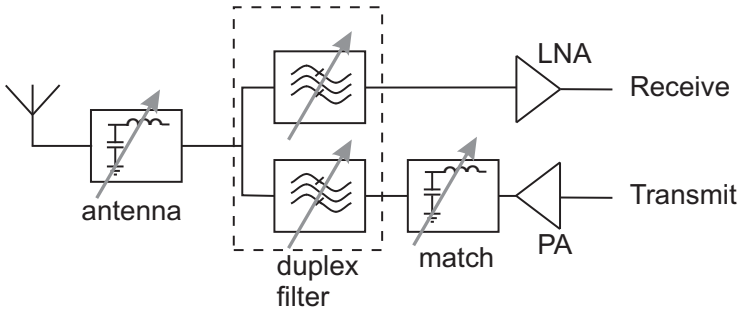


Figure 1.2 – A completely reconfigurable RF front-end.

transmit power than preferred due to the impedance mismatch and the battery will be drained faster. Optimum receive and transmit energy transfer is obtained, with the LNA and PA, through well-designed tunable impedance matching networks.
The matching networks, duplex filter and antenna are ordinarily designed with passive components, such as resistors, coils and capacitors. Tunable resistors [5] and inductors [6] can be used in these applications. However, electrically tunable components in reconfigurable low-voltage RF circuits are typically metal-insulator-metal (MIM) tunable capacitors for many reasons, especially size, cost, and losses [7].

The main work of this thesis is dedicated to thin film ferroelectric MIM capacitors. These devices are also called dielectric varactors or tunable capacitors. The dielectric layer in these capacitors are made of ferroelectric material.
The advantages of implementing the technology of these devices are a low cost, passive integration on cost-effective substrates, the relatively high permittivity of thin ferroelectric films (typically $\varepsilon_\mathrm{r} = 100$–$1000$), and hence its miniaturization potential due to its high capacitance density, continuous (low voltage) tuning (typically $< 40\,\mathrm{V_{dc}}$), integrated decoupling [8], no hermetic packaging, and no moving parts like in MEMS.

1.1 Scope

The first and foremost topic of this work was to study the potential of (low-cost) thin film ferroelectric capacitors for passive reconfigurable RF front-end applications, e.g., matching networks and filters, within a company research and development project. The objectives were to characterize these capacitors at low and high frequencies, give input to further improve the capacitors RF performance, model the measured tuning of a ferroelectric capacitor, and simulate and design test circuits for RF front-end applications. The simulations should give insight on the feasibility of using dielectric varactors in the test circuits.

The research in this work was performed under industrial boundary conditions at the former Philips [9] Semiconductors Research Laboratories and later NXP Semiconductors Corporate Innovation & Technology [10].

1.2 Outline

This thesis starts with a literature study on relevant tunable capacitor technologies in Chapter 2. The trade-off between the quality factor and tuning ratio of tunable capacitors at microwave frequencies has been assessed in terms of basic physics-based models. In Chapter 3, the focus is put on dielectric varactor technology. A brief introduction is given on the basic properties of ferroelectrics with the emphasis on thin film barium strontium titanate. In Chapter 4, the measurement methodology is elucidated and parasitic capacitances and resistances have been discussed. Additionally, an RF measurement technique is elaborated, which can separate the dielectric loss from the resistive electrode loss, indicate process-induced damage and can show the presence of loss-dominating distributed effects. In Chapter 5 work is presented on how to eliminate voltage-dependent AC impedance measurement errors attributed to a wide-band commercial bias-tee by a measurement technique or by using a voltage-independent in-house bias-tee.
In Chapter 6, the potential of barium strontium titanate MIM capacitors is assessed by characterization on alumina and silicon substrates. In Chapter 7, a model of a ferroelectric capacitor is presented which is implemented in a circuit simulator. In Chapter 8, the design of a narrow-band filter and matching networks are discussed. This thesis ends with the conclusions in Chapter 9.

Chapter 2

Tunable technologies in RF applications

2.1 Introduction

In this Chapter, contemporary tunable capacitor technologies are compared to show their potential for reconfigurable cellular applications [11].
A benchmark of tunable and switchable devices at microwave frequencies is presented on the basis of physical limitations. Performance limitations are outlined for each given technology focusing on the quality factor (Q) and capacitive tuning, i.e., tuning ratio (η), as figures of merit, which are defined in Section 3.3. If the performance criteria for the Q and η are not met, the application will not be feasible.
The state of the art in terms of quality factor and tuning ratio of several tunable and switchable technologies is visualized and discussed. Topics such as linearity, power handling and temperature stability are important, but could not be handled on such a general base yet and still require a case by case study.

The following technologies play an important role because of their miniaturization and low-power potential: varactor diodes (varicaps), dielectric varactors, integrated transistor-switched capacitors (CMOS[1], pHEMT[2]), and

[1] Complementary Metal Oxide Semiconductor
[2] Pseudomorphic High Electron Mobility Transistor

micromachined capacitors (RF-MEMS[3]).

The $Q(\eta)$ trade-off at frequencies mainly between 0.5–2 GHz will be discussed for different tunable or switchable devices. In order to beat this trade-off coming up with new ideas could be essential. Simple 1-D device models are employed, assuming the devices are optimized, with key data of the Q and η from literature of each device technology, to present the state of the art.

The devices and technologies are difficult to compare: Measurement conditions and design vary from case to case. $Q(\eta)$ curves for various conditions (breakdown, frequency or voltage) are presented here. However, we give generic comparison figures based on general physical principles wherever possible. The state of the art of the $Q(\eta)$ of each technology will be given in the discussion.

This Chapter is subdivided as follows. In Section 2.2 we discuss the operation principle, the corresponding loss-model and design considerations to improve the device performance with key $Q(\eta)$ data from literature. The lowest quality factor over the tuning range is given throughout this section. In Section 2.3 the state of the art $Q(\eta)$ of each technology is given, compared and discussed. Then, in Section 2.4 the conclusions are drawn. Finally, in Section 2.5 the motivation of why studying the potential of dielectric varactors at RF is addressed.

2.2 Technologies

For each technology in this literature study, parallel-plate capacitors are employed. The parallel-plate capacitance is expressed by

$$C = \frac{\varepsilon_0 \varepsilon_\mathrm{r} A}{h} \tag{2.1}$$

with the permittivity of free space $\varepsilon_0 = 8.85 \cdot 10^{-12}\,\mathrm{F/m}$, relative permittivity ε_r (also in literature indicated as 'kappa' κ) of the dielectric material between the plates, plate area A and the distance h between the plates. The capacitance can be varied

[3]Radio Frequency Micromachined Electro Mechanical System

1. in varicaps via a change in the depletion layer width h_{vc} in the semiconductor,
2. in dielectric varactors through a change in ε_{r},
3. by a combination of switches and capacitors, and
4. in RF-MEMS capacitors by a change in the distance h_{mems} between the two electrodes (planar capacitor) or a change in the effective electrode overlapping area A (comb-like structures), or by a moveable dielectric.

Below, these four approaches are elaborated in detail.

2.2.1 Varicaps

Varicaps or varactor diodes are the most widely used type of electrically continuously tunable capacitors [12]. The capacitance can be tuned by varying the depletion layer width h_{vc} due to a change in DC bias, which is superimposed on an AC signal. A schematic cross-section is depicted in Figure 2.1a, and the loss model is based on the physical operation principle and is shown in Figure 2.1b. The interconnect losses and electrode losses are given by R_{e}, the capacitance of the varicap by C_{vc} and the resistance of the semiconductor by R_{semi}.

An increase in DC bias increases the depletion layer width, which (in case of a Schottky varicap) starts from below the top electrode, reducing the capacitance. The minimum and maximum depletion layer width and the breakdown voltages for silicon (Si) and galium arsenide (GaAs) are calculated using the following formulas in S.M. Sze and K.K. Ng [13] for single-sided abrupt p-n junctions.

The minimum depletion layer width

$$h_{\mathrm{vc,min}} = \sqrt{\frac{2\varepsilon_0\varepsilon_{\mathrm{S}}}{qN}(\psi_{\mathrm{bi}} - \frac{2kT}{q})} \tag{2.2}$$

with ε_{S} the relative permittivity of the semiconductor, the elementary charge $q = 1.6{\cdot}10^{-19}\,\mathrm{C}$, the doping concentration N in cm^{-3}, the built-in voltage $\psi_{\mathrm{bi}} = 0.75$, the Boltzmann constant $k = 1.38{\cdot}10^{-23}\,\mathrm{J/K}$, and the temperature $T = 300\,\mathrm{K}$.

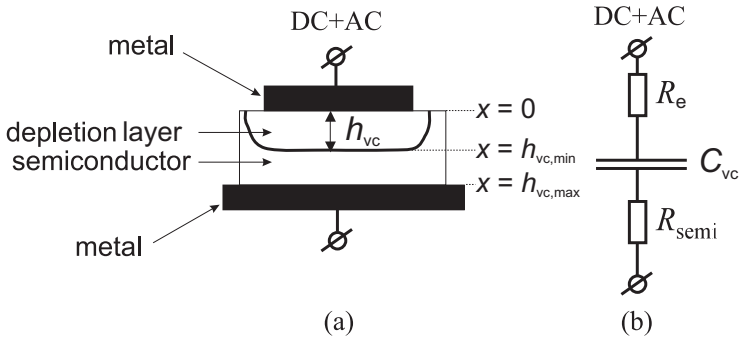


Figure 2.1 – (a) a schematic cross-section of a Schottky varicap. The depletion layer h_{vc} is controlled by the electric field and determines the capacitance value. In (b) the loss-model is shown based on physical operation principles. The interconnect losses and electrode losses are given by R_e, the capacitance of the varicap by C_{vc} and the resistance of the semiconductor by R_{semi}.

The maximum depletion layer

$$h_{vc,max} = \sqrt{\frac{2\varepsilon_0\varepsilon_S}{qN}(\psi_{bi} + V_{rev.,max} - \frac{2kT}{q})} \tag{2.3}$$

with the maximum reverse breakdown voltage $V_{rev.,max}$.

In the case of uniformly doped Si

$$V_{rev.,max,Si} = \frac{E_c h_{vc,max}}{2} = \frac{\varepsilon_0\varepsilon_{r,Si}E^2_{c,vc\ Si}}{2qN} \tag{2.4}$$

with $\varepsilon_{r,Si} = 11.7$, and in the case of GaAs

$$V_{rev.,max,GaAs} = 60(\frac{E_{g,GaAs}}{1.1})^{1.5}(\frac{N}{10^{16}})^{-0.75} \tag{2.5}$$

with $\varepsilon_{r,GaAs} = 12.9$ and the bandgap energy $E_{g,GaAs} = 1.424\,\text{eV}$.

The critical electric field or maximum electric field at breakdown in Si can be described as

$$E_{c,vc\ Si} = \frac{4 \cdot 10^5}{1 - \frac{1}{3}\log_{10}(\frac{N}{10^{16}})} \tag{2.6}$$

for a uniform doping concentration. In general, a non-uniform doping profile is chosen. A heavily doped single-sided, i.e., hyper-abrupt, varicap is often employed [14], which supports a large change in depletion-width and

hence results in a higher Q and η. A large tuning range requires a large change in depletion-width and thus a large series-resistance (low Q due to lowly doped semiconductor) for the minimum depletion state. This trade-off becomes [11, 15]

$$\frac{1}{Q} = \omega C_{\mathrm{vc,max}} R_{\mathrm{semi}} = \frac{\omega \varepsilon_0 \varepsilon_{\mathrm{r}}}{h_{\mathrm{vc,min}}} \int_{h_{\mathrm{vc,min}}}^{h_{\mathrm{vc,max}}} \rho(x) \mathrm{d}x \tag{2.7}$$

with ω the angular frequency, $C_{\mathrm{vc,max}}$ the maximum capacitance of the varicap at $h_{\mathrm{vc,min}}$, R_{semi} the resistance of the semiconductor, and the resistivity of the epi-layer

$$\rho(x) \;=\; \frac{1}{N(x) q \mu_{\mathrm{n}}} \tag{2.8}$$

with the electron mobility μ_{n} in $\mathrm{cm}^2/\mathrm{V{\cdot}s}$ and the depth of the doping profile x. The loss is modeled by interconnect and electrode losses (R_{e}), the resistance of the semiconductor material R_{semi} and by a capacitor (see Figure 2.1b). R_{e} can be minimized by using thick metals and substrate-transfer techniques [16]. R_{semi} is obtained by integrating $\rho(x)$ from $h_{\mathrm{vc,min}}$ to the backside electrode. The well conducting backside electrode should begin at $h_{\mathrm{vc,max}}$. Finally, the dependencies can be inserted in equation 2.10.

Inserting a power-law doping profile

$$\rho(x) \;=\; \rho(h_{\mathrm{vc,min}}) \left(\frac{x}{h_{\mathrm{vc,min}}} \right)^n \;\sim\; x^n \tag{2.9}$$

in equation 2.7 results in

$$Q^{-1} = \omega \varepsilon_0 \varepsilon_{\mathrm{r}} \rho(h_{\mathrm{vc,min}}) \frac{(\eta^{n+1} - 1)}{(n+1)} \quad \text{with} \quad \eta = \frac{C_{\mathrm{vc,max}}}{C_{\mathrm{vc,min}}} = \frac{h_{\mathrm{vc,max}}}{h_{\mathrm{vc,min}}} \,. \tag{2.10}$$

Two special cases, namely $\mathrm{n} = 0$ [17] and $\mathrm{n} = 2$ [15], can be used for low distortion arrangements.

When $n = 0$ a uniform, i.e. abrupt, doping profile is obtained and for $n \gg 0$ a hyper-abrupt doping profile. A hyper-abrupt profile allows for a larger tuning range than a uniform doping profile.
The power-law doping profile enables to study two cases: 1) diodes with low distortions and 2) diodes with different doping profiles. By changing the n, the $Q(\eta)$ of different doping profiles can be studied, so that one can

see how much improvement can be obtained, e.g., by comparing the tuning of an abrupt to a hyper-abrupt diode.
The product $\varepsilon_0\varepsilon_r\rho(h_{vc,min})$ can be regarded as a figure of merit. The (maximum) conductivity $\rho(h_{vc,min})$ is limited by the maximum achievable dopant concentration just before breakdown or tunneling occurs (see further in this section). An excellent value of $\varepsilon_0\varepsilon_r\rho(h_{vc,min}) = 4\,\mathrm{fs}$ seems achievable with very high peak doping levels of up to $10^{18}\,\mathrm{cm}^{-3}$ in Si [15].
Equation 2.10 yields the $Q(\eta)$ function for a given doping profile. The tuning range of a given diode could be traded off for the quality factor if only a part of the tuning range is used, namely between breakdown and a (non-zero) reverse bias.
Another option is to connect a high-quality-factor fixed capacitor in series, as is anyhow needed in many applications which require a bias voltage. In this case the trade-off is of the same form as described by equation 2.10 with $n = 0$ for any doping profile. However, the best trade-off $Q(\eta)$ will be obtained if the dopant concentration is optimized for each maximum tuning ratio η_{max} separately. The following paragraph describes the calculation for abrupt ($n = 0$) Si and GaAs varactors based on the doping dependence of the breakdown field and conductivity.

The conductivity was calculated from the mobility using the empirical model of G. Masetti et al. [18]

$$\mu_n = \mu_0 + \frac{\mu_{max} - \mu_0}{1 + (N/C_R)^\alpha} - \frac{\mu_1}{1 + (C_S/N)^\beta} \tag{2.11}$$

for arsenic doping suited from $N = 10^{13}$– $5{\cdot}10^{21}\,\mathrm{cm}^{-3}$ in Si (highest mobility). The fit parameters $\mu_{0,Si} = 52.2\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$, $\mu_{max,Si} = 1417\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$, $\mu_1 = 43.4\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$, $C_R = 9.68{\cdot}10^{16}\,\mathrm{cm}^{-3}$, $C_S = 3.43{\cdot}10^{20}\,\mathrm{cm}^{-3}$, $\alpha = 0.68$, and $\beta = 2$.
The same model was fitted to the data for GaAs, taken from Figure 18 in reference [13]. The fit parameters are $\mu_{0,GaAs} = 1900\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$ and $\mu_{max,GaAs} = 7600\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$. The remaining parameters to determine the mobility were left constant as in [18].

The results are the dependencies of the quality factor Q and the maximum tuning ratio η on the dopant concentration N, which are parametrically plotted in Figure 2.2 for abrupt Si and GaAs diodes.
Increasing the dopant concentration increases the quality factor, but low-

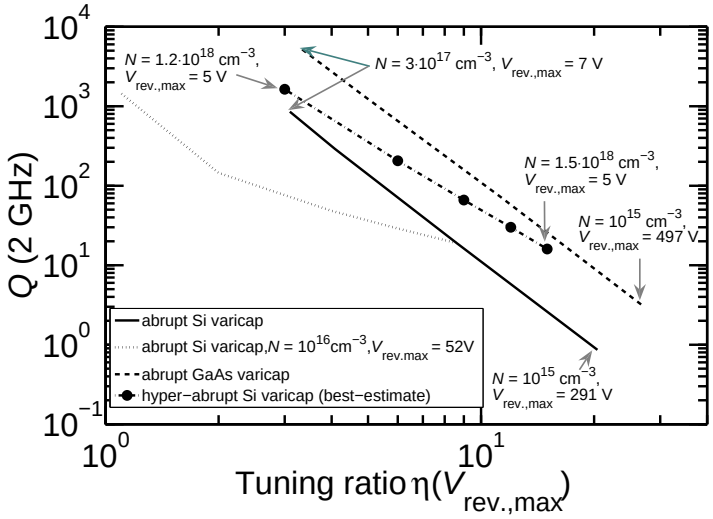


Figure 2.2 – Calculated data of the trade-off between quality factor Q and maximum tuning ratio η for idealized, one dimensional varactor diodes 2 GHz. The solid line denotes abrupt Si varactors, the dashed line abrupt GaAs varactors, and the dash-dotted line hyper-abrupt varactors. The corresponding dopant concentrations N and reverse breakdown voltages $V_{\mathrm{rev.,max}}$ are attached to selected points on the lines. The dotted line shows an abrupt Si varactor with fixed dopant concentration of $10^{16}\mathrm{cm}^{-3}$, where only a part of the tuning range is used by demanding a minimum bias voltage.

ers the breakdown voltage and hence the tuning range. If the dopant concentration is very high, tunneling can occur at the junction, so that the tuning range is further reduced. In Si(Ge) this will occur above $N > 3{\cdot}10^{17}\,\mathrm{cm}^{-3}$ [19]. The curves are therefore plotted till this level. The lowest dopant concentration was chosen so that Q was in the range of 1–10. The calculated $Q(\eta)$ data for Si is close to what is postulated by the International Technology Roadmap for Semiconductors from 2012 on [20]: $Q > 50$ at 5 GHz (corresponds to $Q > 125$ at 2 GHz) for $\eta > 5.5$.

The functional dependence of $Q(\eta)$ from equation 2.10 can be approximated by $1/Q \sim \eta^{n_\mathrm{a}+1}$ with $n_\mathrm{a} = 2.6$ for Si for $\eta \approx 4$–10 and $n_\mathrm{a} = 2.67$ for GaAs for $\eta > 4$, with '$n_\mathrm{a} + 1$' the relevant slope in Figure 2.2. The doping dependence of the mobility has been obtained by fitting it with a power law and assuming large tuning ratios. It should therefore fit best to low dopant concentrations. Although in equation 2.10 the optimization of the breakdown voltage has not been taken into account, it can fit the results by using a modified exponent

$n \approx 2.6$ instead of $n = 0$ for abrupt varactor diodes. This confirms that optimizing a diode for the needed tuning range is better than reducing the tuning range by using only a part of the $C(V)$ curve. The second case is also plotted in Figure 2.2.

Hyper-abrupt varactor diodes can be optimized for the maximum tuning range not only by the doping level, but also by the shape of the doping profile. Such a study was undertaken by C. Huang et al. for $n = 2$ [15]. The best reported values for a constant reverse breakdown voltage of 5 V are plotted in Figure 2.2. All data points have a maximum dopant concentration of ca. $10^{18}\mathrm{cm}^{-3}$ at the junction. A higher reverse voltage does not necessarily lead to a better $Q(\eta)$ trade-off for the higher tuning ratios [15]. The resulting $Q(\eta)$ curve can also be fitted by equation 2.10 with $n \approx 2$ and $\varepsilon_0 \varepsilon_\mathrm{r} \rho(d_\mathrm{min}) \approx 4\,\mathrm{fs}$.
Hyper-abrupt varactors can have a better $Q(\eta)$ trade-off, but the functional shape of the trade-off is similar to that of abrupt Si diodes. The performance of hyper-abrupt GaAs varactor is expected to be higher than that of Si, analogous to abrupt varactor diodes. It should be noted that for high quality factors ($Q > 100$) additional losses from the electrode connections become important.

2.2.2 Dielectric varactors

Another type of continuously tunable capacitors is the dielectric varactors. The permittivity changes when a voltage is applied to the capacitor. This varactor is the smallest tunable capacitors due to its high permittivity, e.g, the ε_r of a semiconductor material (≈ 12) is typically much smaller than the ε_r of a ferroelectric material (typically > 100). The parallel plate metal-insulator-metal (MIM) capacitor (see Figure 2.3) has low fringing fields, a high capacitance density and a low tuning voltage [7].

The relative permittivity of some materials, notably those with a high permittivity like ferroelectrics, e.g., $\mathrm{Ba_xSr_{1-x}TiO_3}$ (BST), changes by applying a non-zero DC bias field due to the saturation of the dielectric polarization [21]. A higher electric field decreases the permittivity.
Non-ferroelectric, but nevertheless tunable dielectrics with a high permittivity exist, e.g., with a pyrochlore phase like $\mathrm{Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7}$ (BZN). Liquid crystals are representative for a tunable dielectric with a low dielectric constant [22]. However, their tuning ratio is limited to the low

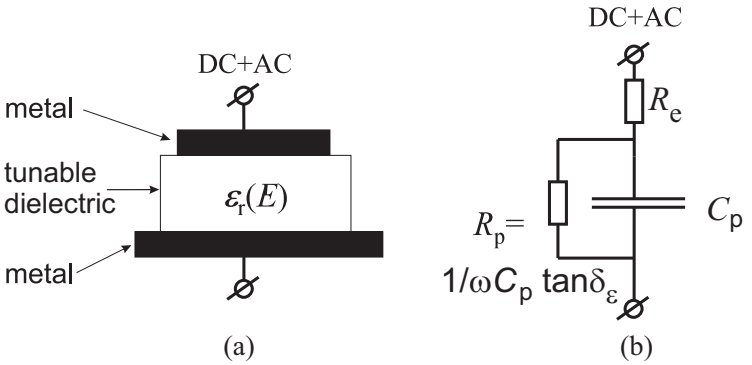


Figure 2.3 – Part (a) shows the schematic cross-section of a metal-ferroelectric-metal capacitor. A change in electric field E between the parallel metal plates changes the ε_r of the ferroelectric. In (b) the loss-model is shown. The series resistance of the interconnect loss and electrodes is given by R_e, the resistivity of the dielectric by R_p and the ferroelectric capacitance by C_p.

maximum relative permittivity. The tuning ratio in these components is $\varepsilon_{r,max}/\varepsilon_{r,min}$ [23].

The capacitance of the tunable dielectric C_p is not ideal. The dielectric loss $\tan\delta_\epsilon$ (see Section 3.3), and the interconnect and electrode resistance (R_e) cause dissipation (Figure 2.3). The series resistance of the interconnects can be minimized by small patterns and thick metals with a high conductivity. The latter also holds for the electrodes.
Ferroelectric materials are mainly used in their paraelectric state in the temperature region above the Curie temperature [24], because of lower losses. The tuning ratio in the ferroelectric phase, which exists in the temperature region below the Curie temperature, is higher, at the cost of higher losses due to irreversible domain wall movements [24, 25].
Since ferroelectric materials have piezoelectric or electrostrictive properties [24], a bulk acoustic wave [26, 27] is excited when a DC electric field is applied [28]. The layers of the capacitor should be chosen in such a way that the acoustic wave is suppressed at the operating frequency. Alternatively the materials can be used for acoustic filters [29], which could even be tunable [30–33].

The high non-linear permittivity of most tunable dielectrics is caused by atomic displacements [34]. Acoustic losses due to the phonon excitation by the atomic movements are the limiting (intrinsic) loss factor [23]. First, a simple model for the intrinsic losses is given. Then a phenomenological $Q(\eta)$

is proposed based on literature data that includes extrinsic losses, e.g., by defects in the thin layers.
Assuming a bias-field-induced Quasi-Debye mechanism for the intrinsic losses a trade-off

$$Q^{-1} = \omega\tau_{\mathrm{d}}(\eta - 1), \text{ with } \tau_{\mathrm{d}} = A_{\mathrm{deb}} I_{\mathrm{deb}}(E_0) \tag{2.12}$$

can be derived between the quality factor Q and the tuning ratio η [23, 35]. The angular frequency ω should be well below the phonon damping frequency (ca. 100 GHz) [23, 35]. The parameter I_{deb} [23, 35] depends on the tuning field E_0 and is in the order of 1 for small fields (tuning ratio η close to 1). The parameter A_{deb} is expected to be in the order of magnitude of 1000 fs [23, 35]. The measured literature data from Figure 2.4 above 1 GHz correspond to values of $\tau_{\mathrm{d}} = 100$–2000 fs.
Equation 2.12 predicts the highest losses at high tuning field, because then the acoustic coupling is strongest. Single crystalline materials often follow this behavior. However, many thin film measurements show the opposite dependence. The losses are lowered at high fields. Defects, stress distributions, interfaces or a resistive electrode design are possible causes for this behavior.
In general, careful processing measures should be taken to minimize bad interface layers to the film, porosity and cracks, which could decrease Q. A thin dead layer (an unintentional low ε_{r} dielectric layer between 1 or more electrodes and the high ε_{r} ferroelectric layer) also reduces the tuning ratio. The capacitive test structures should be small in physical size to increase the Q of high permittivity ferroelectric capacitors, as discussed in [36].
The capacitance and quality factor are frequency dependent due to dielectric relaxation (see Chapter 3). The relaxation current density J_{r} versus time t of real ferroelectric devices after a voltage step follows a power-law dependence, denoted as the Curie-von Schweidler behavior [37, 38], which can be expressed as

$$J_{\mathrm{r}}(t) \;=\; J_0(E) \cdot t^{-(\beta+1)} \tag{2.13}$$

with $J_0(E)$ a field-dependent parameter, and with $0 < \beta < 1$. The time-dependent polarization relaxation exhibits itself as the dispersion in quality factor with respect to frequency [39]

$$Q \sim \omega^{-\beta}, \tag{2.14}$$

a less severe frequency dependence than predicted by a Debye model [37]. Limited experimental data for BST and BZN show frequency dependencies β even below 0.1–0.33 [38, 40, 41]. Therefore a phenomenological approach was chosen.

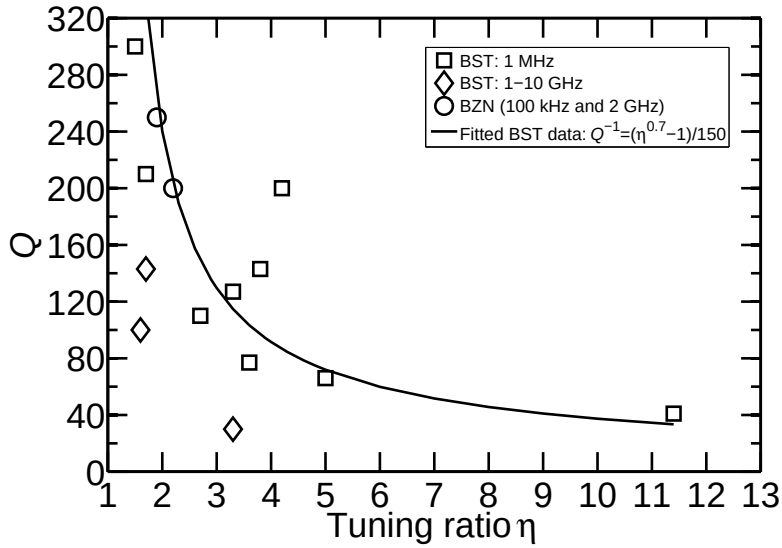


Figure 2.4 – The results are based on a literature survey on the performance of dielectric parallel plate MIM varactors in terms of Q and η. The solid line is a fit to the best reported measurement results of ferroelectric varactors ($Ba_xSr_{1-x}TiO_3$ (BST), squares) at 1 MHz [40–48]. Data of BST for 1–10 GHz are plotted as diamonds [40, 41]. The $Q(\eta)$ literature data of varactors based on the non-ferroelectric dielectric BZN are indicated by circles [49, 50]. The BST data indicate that Q decreases when η increases.

Data on thin film ferroelectrics, using different deposition techniques, which have resulted in a high tunability and low losses were collected for parallel plate MIM capacitors at 1 MHz for $Ba_xSr_{1-x}TiO_3$ (BST) [40–48]. Data of BST between 1–10 GHz is given in [40] and [41]. For the non-ferroelectric dielectric BZN, data is indicated in [49, 50]. Many more papers exist on microwave losses in thin dielectric films, but only papers were chosen with the best $Q(\eta)$ values of parallel plate MIM capacitors with electrodes that are realistic for miniaturized devices.

If the assumption is made that the losses of dielectric varactors will only slightly increase with frequency following a Curie-von Schweidler law after Fourier transform (see equation 2.14), then the low frequency results pose an upper limit to the high frequency performance (see Figure 2.4).
Experimental results show a weaker dependence of Q on η than equation 2.12 predicts. We attribute the difference to the significance of extrinsic losses in polycrystalline material.

The low frequency $Ba_xSr_{1-x}TiO_3$ data can be fitted by

$$Q^{-1} = (\eta^{0.7} - 1)/150 \tag{2.15}$$

(see Figure 2.4). Data at microwave frequencies in some cases come close to the low frequency data. This is another indication that the losses are still dominated by extrinsic losses and less by intrinsic losses as described by equation 2.12.
The $Q(\eta)$ plot shows the limiting (fitted) curve of what could be achieved if the tuning field is increased up to breakdown. The data suggests there is still room for improvement by reducing the extrinsic defects.

2.2.3 Semiconductor-switched capacitors

Semiconductor components such as PIN-diodes, CMOS switches and pHEMT switches offer high performance at RF frequencies. PIN-diodes dissipate considerable power in the on-state and are therefore left out in this study, although they can have a good high-frequency performance.

A transistor-switched capacitor is basically a transistor in series with a non-tunable (linear) capacitor or a tunable capacitor (see Figure 2.5).

In Figure 2.5 the drain-source capacitance is expressed as C_{ds}, the source-gate capacitance as C_{sg}, and the drain-gate capacitance as C_{dg}. The off capacitance is expressed as [52]

$$C_{\mathrm{off}} = \frac{C_{\mathrm{sg}}C_{\mathrm{dg}}}{C_{\mathrm{sg}} + C_{\mathrm{dg}}} + C_{\mathrm{ds}}. \tag{2.16}$$

Typically, a non-tunable MIM capacitor is used due to its higher Q-factor. High-quality MIM capacitors are available that have negligible small losses with respect to the losses of the switch. Such capacitors have dielectrics

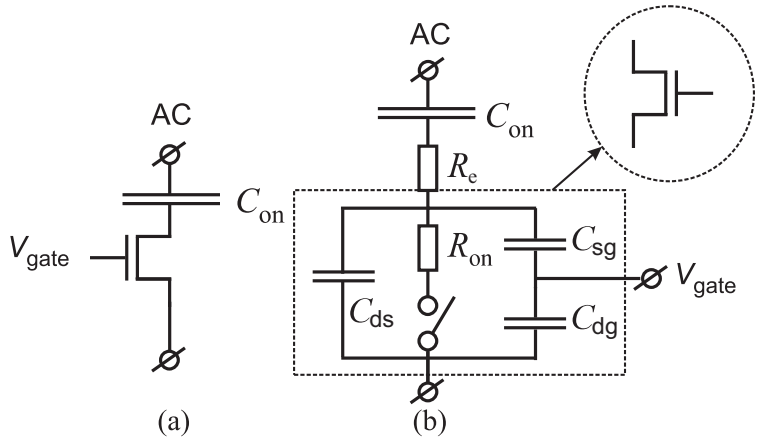


Figure 2.5 – In (a) a schematic picture of a transistor in series with a capacitor is given. If sufficient gate bias V_{gate} is applied on the transistor, a channel is formed between the source and drain, and the capacitor is connected to the circuit [51]. In (b) the loss-model of the transistor-switched capacitor is depicted [51, 52]. When the switch is closed, R_{on} dominates the performance. When the switch is open, the off-capacitance C_{off} (see equation 2.16) dominates the minimum capacitance. The capacitance C_{on} is assumed to be an ideal capacitor, e.g., a low loss MIM capacitor.

with a low dielectric constant and low losses, such as SiO_2, Si_3N_4 or Al_2O_3 and are connected with highly conducting electrodes such as, e.g., Al or Cu. The transistor is employed to switch a capacitor on/off. In the off-state the parasitic capacitance of the switch determines the minimum capacitance value. In the on-state the transistor resistance determines the Q of the switch-capacitor configuration.
We assume that the switch is connected to an ideal capacitor. Varying its value yields the trade-off between the tuning ratio η and the quality factor Q in the on-state. In the model presented in Figure 2.5 the on-state yields a lower Q than the off-state, so that we take the lower value in the on-state for the comparison. A low on-resistance R_{on} is thus crucial for a high Q switched capacitor array.

In this section, we discuss CMOS and pHEMT switches. We assume $R_{\text{on}} \gg R_{\text{e}}$. The $Q(\eta)$ trade-off for CMOS and pHEMT switches becomes

$$Q^{-1} = \omega R_{\text{on}} C_{\text{off}} (\eta - 1)\,, \tag{2.17}$$

which is the same expression as for uniformly doped varicaps. Equation 2.17 is utilized to plot literature data from

1. CMOS switches, on 0.13 μm Si at 0.7 GHz [53], on 0.18 μm Si at 2.4 GHz [54], on 0.18 μm silicon-on-insulator (SOI) at 2 GHz [55] and on 0.5 μm silicon-on-sapphire (SOS) [51], and

2. pHEMT switches, on 0.5 μm GaAs at 2 GHz [51], and on 0.15 μm and 0.5 μm GaAs at 0.9 GHz [52]

in Figures 2.6 and 2.7, respectively. The best figures of merit $R_{\mathrm{on}}C_{\mathrm{off}}$ are reported for the case of a 0.5 μm CMOS-switch on Sapphire $R_{\mathrm{on}}C_{\mathrm{off,CMOS}} = 750$ fs [51] and a 0.5 μm pHEMT switch $R_{\mathrm{on}}C_{\mathrm{off,pHEMT}} = 360$ fs [56].

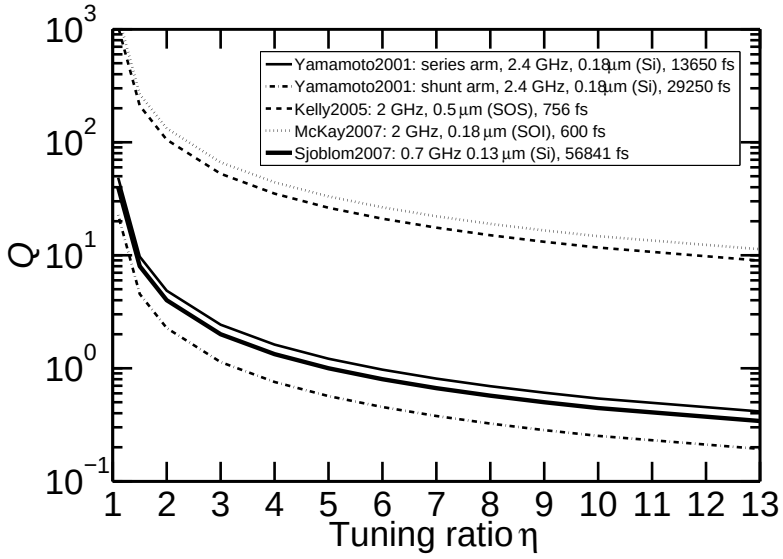


Figure 2.6 – The performance of CMOS switches in terms of Q and η at 0.7 GHz (0.13 μm Si, $R_{\mathrm{on}}C_{\mathrm{off}} = 56841$ fs [53]), 2 GHz (0.18 μm SOI, $R_{\mathrm{on}}C_{\mathrm{off}} = 600$ fs [55] and 0.5 μm SOS, $R_{\mathrm{on}}C_{\mathrm{off}} = 756$ fs [51]) or 2.4 GHz (0.18 μm Si, $R_{\mathrm{on}}C_{\mathrm{off}} = 13650$ fs (series arm) and 29250 fs (shunt arm) [54]) based on a literature survey. The experimental data from literature are for Si, silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) substrates. The products of $R_{\mathrm{on}}C_{\mathrm{off}}$ of the CMOS switches from literature are filled in equation 2.17, which results in the curves above. The Q decreases with increasing η.

In CMOS switches N-channel MOSFETS are preferred because of a low R_{on}. The width of the channel needs to be optimized [57]. A large width

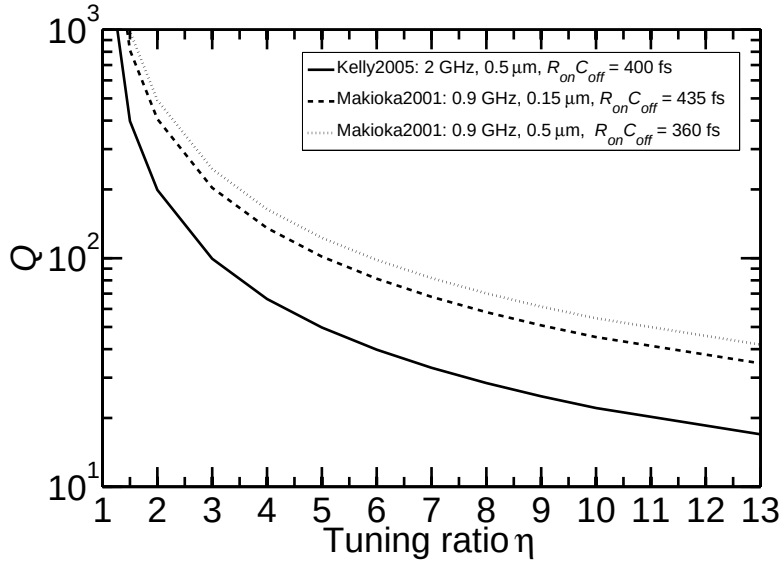


Figure 2.7 – The performance of pHEMT switches in terms of Q and η at 0.9 (0.15 μm and 0.5 μm [52]) or 2 GHz (0.5 μm [51]) based on equation 2.17 and a literature survey. The measurement results from literature are performed on Si, silicon-on-sapphire (SOS) and on SOI substrates. The product of $R_{\mathrm{on}}C_{\mathrm{off}}$ shown in the Figure are filled in equation 2.17 which results in the curves above. The Q decreases with increasing η.

reduces R_{on} and increases Q to a certain extent. When the width becomes too large, then the capacitive coupling to the substrate reduces Q.

In pHEMT switches the channel doping decreases the R_{on} at the cost of additional parasitic capacitance between the source and drain reducing the isolation in the off-state [58].

2.2.4 RF-MEMS

RF-MEMS [59] contain movable parts and can be configured as miniaturized (galvanic) relays or continuously tunable capacitors. These switches have a relatively large physical size [60], compared to the other devices discussed earlier, due to the actuator that moves the mechanical parts. Galvanic RF-MEMS switches are similar to semiconducting switches and will be briefly discussed at the end of this section. In capacitive RF-MEMS switches the geometry of a capacitor is varied. A compact version, although still relatively

large compared to other tunable technologies, e.g., ferroelectric capacitors, due to the low ε_r, is a planar electrostatic RF-MEMS capacitive switch, where the RF capacitor is also the electrostatic actuator (see Figure 2.8).

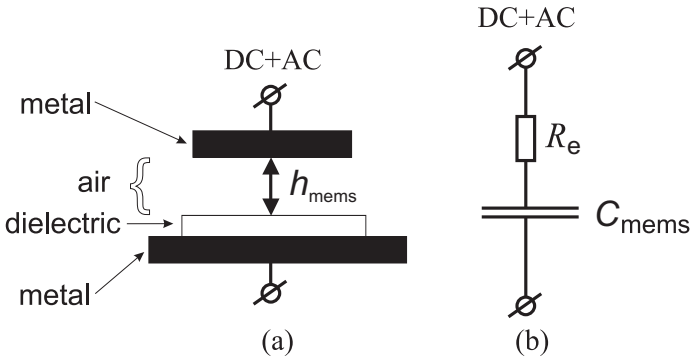


Figure 2.8 – In (a) the schematic cross-section of a planar RF-MEMS electrostatic switched capacitor is shown. The dielectric layer prevents a short-circuit between the top electrode and the bottom electrode. The distance h_{mems} between the top electrode and the dielectric determines the value of the capacitance and is controlled by the electric field. In (b) the loss-model is given and is based on physical operation principles. The interconnect and resistive electrode loss is given by R_e and the capacitance of the planar RF-MEMS capacitive switched capacitor by C_{mems}.

The capacitance is tunable by varying the distance h_{mems} between the top electrode and the dielectric, by a DC bias stimulus superimposed on an AC signal, or by a separate actuator. This principle also holds for vertical 3D MEMS like comb-structures. The combs move in-plane and vary the overlap area of the electrodes.

IDC capacitors in MEMS technology have low parasitic capacitances due to the use of air as a dielectric, and the interdigitated fingers have a very large aspect ratio, so that they become 90-degree tilted 'MIM capacitors'. Rotational movement like in manual trimming capacitors is less suited for integration on wafer level due to a lack of bearings, but can be integrated vertically [61].

J-B. Yoon and C.T.-C. Nguyen [62] designed an RF-MEMS, which can move a dielectric horizontally between two parallel plates. Measurements on prototypes of this design show a Q of 218 at 1 GHz with a tuning range of 40 % ($\eta \approx 2$). The 'movable dielectric' devices are limited in tuning range due to the air gap.

There is no fundamental difference in gap tuning, area tuning and move-

able dielectric tuning, since the dielectric layer (air or vacuum) is basically lossless and the electrode and anchor losses dominate performance of unpackaged planar RF-MEMS capacitively switched devices. In principle, the planar RF-MEMS capacitive switched capacitor has no trade-off between quality factor and tuning ratio. But it has practical limitations. The equivalent circuit is shown in Figure 2.8.

The dielectric losses for common insulators, in planar RF-MEMS electrostatic capacitive switches, such as SiO_2 and Si_3N_4 are negligible ($\tan\delta < 0.003$ is certainly feasible). The main losses therefore come from the resistive electrodes, whereas in the other discussed technologies the inherent losses add to, or often dominate over the electrode losses.

The trade-off between a practical actuator and the capacitor design induces a trade-off between Q and η. One of the typical bottlenecks are the electrode connections to the movable electrode ('anchors'). They need to be well conductive, but at the same time they must be flexible to allow movements. H.S. Lee et al.[63] circumvented this by using an electrically floating top plate and two separate planar bottom plates. Two capacitors are measured in series from the floating top plate to the bottom plates. The signal pad goes via the substrate without passing through the mechanical springs. The capacitance varies between 300–430 fF, $Q \approx 70$ at 2 GHz and $\eta = 1.7$ at 5 GHz.

Smaller planar RF-MEMS capacitive switches need narrower or thinner connections when the tuning ratio and the actuation is kept constant. But it also has a lower capacitance, so that the quality factor is not strongly dependent on the size of the planar capacitive RF-MEMS switch, but rather on the gap that needs to be closed. A larger gap yields a higher anchor resistance at a given actuation voltage. A large gap is equivalent to a large tuning ratio. The electrode surface roughness additionally affects the maximum capacitance when closed ($C_{\max}$) and should be low [64] to yield a high tuning ratio.

Parasitic effects, such as coupling to the substrate, are of course also important and are normally strongly reduced by isolating substrates. For a best estimate those effects are neglected here. Then R_e and $C_{\mathrm{MEMS,max}}$ are the crucial parameters and the quality factor is expressed by

$$Q^{-1} = \omega R_e C_{\mathrm{mems,max}} = \omega R_e C_{\mathrm{mems,min}} \eta \tag{2.18}$$

with the resistance R_e of the electrodes. The measurement data from literature [61, 63, 65–68] differ in some cases from 2 GHz, but are in the range of 0.5–5 GHz.

A Q of 300 has been measured at 2 GHz with a tuning ratio of 8 at a maximum actuation voltage of 17 V and a nominal capacitance of 0.47 pF [68], yielding $R_e C_{mems,min} = 33$ fs. The data from literature in combination with equation 2.18 give a benchmark for planar RF-MEMS capacitive electrostatic switches.

The RF-MEMS electrostatic capacitive switch shows a high Q across the tuning range at 2 GHz. The trade-off between the Q and η for these devices are visualized in Figure 2.9 for gap-tuned capacitive RF-MEMS devices, since these devices uphold the highest performance.

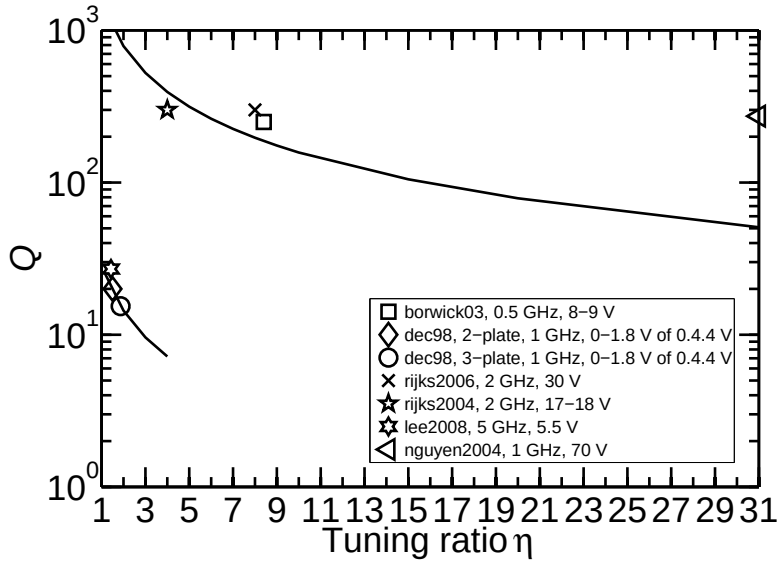


Figure 2.9 – The results are based on equation 2.18 and a literature survey on the $Q(\eta)$-performance of planar RF-MEMS electrostatic capacitive switches between 0.5–5 GHz [61, 63, 65–68]. The actuation voltage, and operating frequency differs in some cases from 2 GHz since not all measurements in literature are performed the same. Measured data points of capacitive RF-MEMS devices using the gap tuning principle are shown; except for 'nguyen2004' [61] which uses vertical comb-driven angular capacitors with fairly large actuators. Two trendlines are indicated for lower and higher actuation voltages. The Q decreases with increasing η.

The performance close to $Q = 20$ shows that the Q decreases with η. Planar RF-MEMS capacitive switches with a higher $Q(\eta)$ performance close to

$Q = 300$, also show the same decrease. Two trendlines have been drawn for both groups of datapoints.
Galvanic RF-MEMS switches make or break an Ohmic contact as a relay. Their equivalent circuit can be compared to the simplified model for semiconducting switches in Figure 2.5. An ideal fixed capacitor is connected to the galvanic MEMS switch. The on-resistance is a sum of the resistance of the anchors and the resistance of the contact. A capacitive RF-MEMS switch with the same size of a galvanic RF-MEMS switch can therefore have a lower series resistance. But on the other side there is the advantage of a lower off-capacitance because of the small contact area.
The size of the galvanic MEMS is mainly determined by the size of the actuator. A large actuator can induce a high contact force and ensure a low on-resistance. A trade-off on the size of the switch is therefore expected. This is also reflected in Figure 2.9. A lower actuation voltage or smaller size leads to a higher loss.
One of the best reliable galvanic MEMS switches [69], which is still fairly large, achieves a figure of merit of $R_{\mathrm{on}}C_{\mathrm{off}} \approx 30\,\mathrm{fs}$. This is in the same order of magnitude as planar capacitive RF-MEMS and clearly demonstrates the performance potential of planar RF-MEMS capacitive switches.

2.3 Discussion

The state of the art performance in terms of $Q(\eta)$ of each tunable and switchable technology is combined and summarized in Figure 2.10. Experimental $Q(\eta)$ results of dielectric parallel plate varactors are fitted. For varactor diodes the limiting simulations are given.

For practical reasons a transistor-capacitor switchable array is preferred in the high tuning regime (including parasitics) and best realized by pHEMT and CMOS. Although, RF-MEMS capacitive switches offer even a higher tuning ratio, they are less mature and less widely available. For the lower tuning ranges diodes offer higher performance. The values of CMOS and pHEMT switches are somewhat worse compared to varicaps due to the parasitic capacitances at the channel.
RF-MEMS capacitive switches offer a low loss with a high tuning ratio as well as digital operation. For the latter, a large physical size and a relatively small capacitance value, due to hermetic packaging constraints,

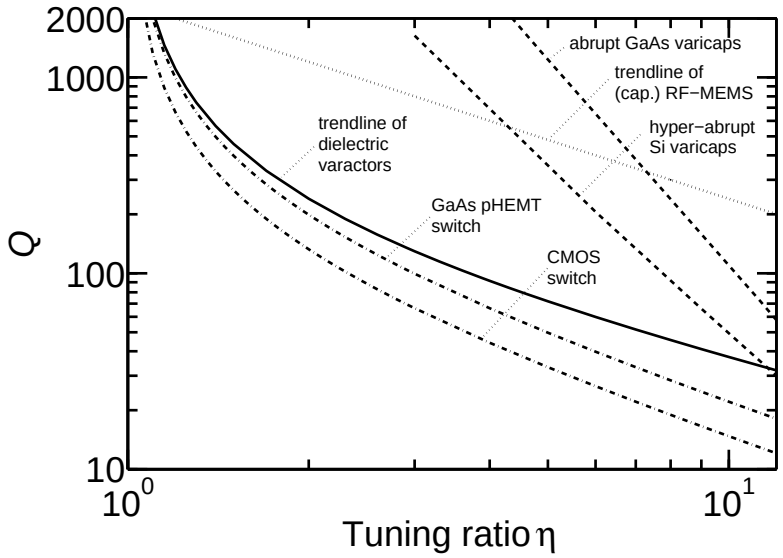


Figure 2.10 – The state of the art intrinsic quality factor Q at 2 GHz without interconnects versus the tuning ratio $\eta = C_{\max}/C_{\min}$ limited to $\eta = 12$. All data are given at 2 GHz unless stated otherwise. The best data found in literature for GaAs pHEMT (0.5 μm) [51] and CMOS(0.18 μm SOI) switch [55] are shown with dash-dotted lines.
The solid line is a fit to the best reported measurements of ferroelectric varactors ($Ba_xSr_{1-x}TiO_3$) at 1 MHz. The trend line also overlaps the data points of non-ferroelectric $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ at 100 kHz and 10 GHz. The dashed lines represent the $Q(\eta)$ response of ideal abrupt GaAs varicaps with $N = 10^{15}$–$3{\cdot}10^{17}$ cm^{-3} and respectively $V_{\text{rev.,max}} = 497$–$7$ V, and the best-estimate of a hyper-abrupt Si varicaps with $N = 10^{18}$ cm^{-3} at $V_{\text{rev.,max}} = 5$ V [15].
The dotted line is the trendline for higher actuation voltages for planar RF-MEMS electrostatic capacitive switches assuming that the loss and tuning are proportional to the maximum capacitance [68].

results in a limited capacitance density. J-B. Yoon and C.T.-C. Nguyen [62] who designed and measured on a MEMS device with a movable dielectric in between the plates, obtained experimental Q(eta) values which are not higher than we report in Figure 2.9. Therefore the reasoning that 'practical' devices, useful for applications, will have a trade-off still remains valid. There is no trade-off - as already stated - if the actuator can be as large as pleased.

The present state of the reliability of capacitive and a galvanic RF-MEMS switches for upcoming military and commercial applications is presented in [70].

The differences in the quality factor Q at tuning ratios below 3 become less important if the capacitors are combined with a coil. A coil typically has a Q-factor below 100 at 1–2 GHz, especially when integrated or miniaturized. The choice then depends more on other features such as size, cost and availability.

Finally, the described trade-offs can be approximated by:

$$Q^{-1} = (\omega\tau)^{\beta}(\eta^{n+1} - 1)/(n+1) \tag{2.19}$$

In most cases β equals 1, except for some extrinsic dielectric losses that scale with $\beta < 1$. The exponent n is a measure on how fast the quality factor drops with increasing tuning ratio η. It can be influenced by the device design, but is normally larger than 1. The state of the art performance of the discussed tunable technologies is depicted in Table 2.1.

Device	*State-of-the-art performance*	*Equation*	*Comments*	*Ref.*
Varicap				
Abrupt (GaAs)	$n = 0$, $\beta = 1$, $\tau = \varepsilon_0\varepsilon_r\rho = 967$ fs	2.10	2 GHz	[16]
Hyper-abrupt (Si)	$n = 2$, $\beta = 1$, $\tau = \varepsilon_0\varepsilon_r\rho =$ 4-6 fs	2.10	2 GHz, $V_{\mathrm{rev.,max}} = 5$ V, modeled	[15]
Dielectric Varactor	$n \approx 0$, $\beta < 1$, $\tau_d =$ 100–2000 fs	2.19	2 GHz, see caption	[11]
switched C				
CMOS (0.18 μm SOI)	$n = 0$, $\beta = 1$, $\tau = R_{on}C_{off} = 600$ fs	2.17	2 GHz	[55]
pHEMT (0.5 μm GaAs)	$n = 0$, $\beta = 1$, $\tau = R_{on}C_{off} = 400$ fs	2.17	2 GHz	[51]
capacitive RF-MEMS	$n = 0$, $\beta = 1$, $\tau = R_eC_{min} = 33$ fs	2.18	2 GHz	[68]

Table 2.1 – The state-of-the-art performance τ from equation 2.19 is listed together with the exponent n in the $Q(\eta)$ trade-off. The value for the dielectric varactors is based on measured high frequency data for low tuning ratios and projections based on low frequency measurements.

Circuit designs with external low-loss capacitors therefore will not improve the $Q(\eta)$ trade-off significantly.
Additionally, the series connection increases the breakdown voltage, but the trade-off $Q(\eta)$ remains. For example, increasing the dielectric thickness of

the same ferroelectric MIM varactor will increase the breakdown voltage, but will not change the Q(η) trade-off that is fixed by the material properties of the dielectric film.
Switches can also be connected in series for higher breakdown voltage, but normally at the cost of additional parasitics. Power handling from, e.g., a $3\,V_{\mathrm{dc}}$ battery can be increased with voltage converters (see, e.g., [71]). However, a low operation voltage lowers the cost and size, and makes the device more attractive for an application.
It should be stated that the above discussion outlines the general trend for the intrinsic performance. Packaging and interconnects can degrade the performance severely and must be optimized for each of the technologies within the given (cost) constraints. When a high linearity is required and higher power handling, many tuning devices can be connected in series [72, 73], which is only attractive for small devices. Switched capacitors have advantages when linearity is a priority, whereas continuously tuned devices are typically smaller than arrays of switches.

2.4 Conclusions

The trade-off between losses and tuning ratio of tunable capacitors at microwave frequencies has been assessed in terms of basic physics-based models. All technologies show an increased loss for higher tuning capability and can be approximated by an equation $Q^{-1} \sim (\eta^{n+1} - 1)$ with $n =$ -0.3–2. Planar micro-electro-mechanical capacitive switches have the highest tuning potential with a high Q, but are large. For continuous, moderate tuning ranges $\eta < 3$, highly doped GaAs varactor diodes could offer the best performance. Ferroelectric capacitors will be an alternative if small physical size and low cost processing are mandatory.

Besides showing the limitations of some tunable technologies, new emerging tunable technologies like tunable electro-acoustic resonators (surface acoustic waves (SAW) [74], bulk acoustic waves (BAW) [26]) are getting more attention from the research community. Acoustic waves are generated if an electric field is applied to the input port of a device containing a piezoelectric material. The electrical energy is transformed into mechanical energy [25], after which an acoustic wave is excited in the piezoelectric material resulting in a resonance. A high Q resonator in the microwave range can be obtained

if the electrode loss, the acoustic wave leakage and the mechanical loss are low [75]. However, a large tuning of the resonance frequency still remains a challenge, e.g., for $SrTiO_3$ less than 2 % [31, 76, 77], $Pb(Zr_xTi_{1-x})O_3$ (PZT) more than 3 % [30], or ZnO [78].

2.5 Focus on dielectric varactors

In this work was opted for dielectric varactors as a tunable technology. Before the start of this work, ferroelectric capacitors were optimized within the company for low-frequency applications, using wet-chemical processing of lead zirconate titanate (PZT) thin films, and are currently being mass-produced, yielding a high throughput, in combination with semiconductor factory-compatible materials.
Ferroelectric capacitors in this work are based on a different ferroelectric material used for RF applications and enable a cost-effective approach (small physical area consumption, passive integration on cost-effective substrates, no hermetic package, relatively fast wet-chemical processing, processing experience exist within the company, and re-use of semiconductor factory fabrication equipment).

The potential at RF was assessed, based on a number of important pillars:

1. reconfigurable continuous (low-voltage) tuning (typically $< 40\,V_{dc}$),
2. high capacitance density (typically $\varepsilon_r = 100$–1000, small physical area, thin films, integrated decoupling [8]),
3. a good temperature stability of the ε_r is feasible, and
4. no moving parts.

In Chapter 3 an introduction is given on dielectric varactors, i.e., ferroelectrics, with the focus on thin film barium strontium titanate films.

Chapter 3

Ferroelectric materials and properties

3.1 Introduction

This Chapter summarizes the most important aspects of ferroelectric materials, as an introduction to the studies on BST-based capacitors presented in the remainder of this thesis.

Ferroelectrics are a class of dielectrics with a spontaneous polarization, which can be reversed in an electric field [25]. Dielectric materials are insulators. In capacitors the dielectric layer is located in-between two electrodes. Unlike conventional dielectrics used in the integrated circuit technology, e.g., SiO_2, Si_3N_4 or Al_2O_3, the relative permittivity ε_r of ferroelectric material is a nonlinear function of the electric field E.
An applied voltage results in an orientation of the polarization in the electric field E. The polarization P in ferroelectrics is remnant after the applied voltage is removed, is reversible, and saturates with increasing $|E|$ [79]. The ε_r of a capacitor can be obtained from non-hysteretic $P(E)$ curves by calculating the susceptibility χ, i.e., the slope of the curve at each measured E [79]. Successively, the $\varepsilon_r(E)$ can be computed by

$$\varepsilon_r(E) = 1 + \chi(E) \tag{3.1}$$

at a constant operation temperature T.

The $P(E)$ curves of a linear capacitor, and that of a nonlinear ferroelectric capacitor in the ferroelectric and the paraelectric phases are depicted in Figure 3.1 with a brief summary of various properties of the two crystal phase structures given in Table 3.1. A single material can exhibits two crystal phase structures. In this dissertation the material will be named a ferroelectric capacitor, even if the temperature response is studied at in the paraelectric phase.

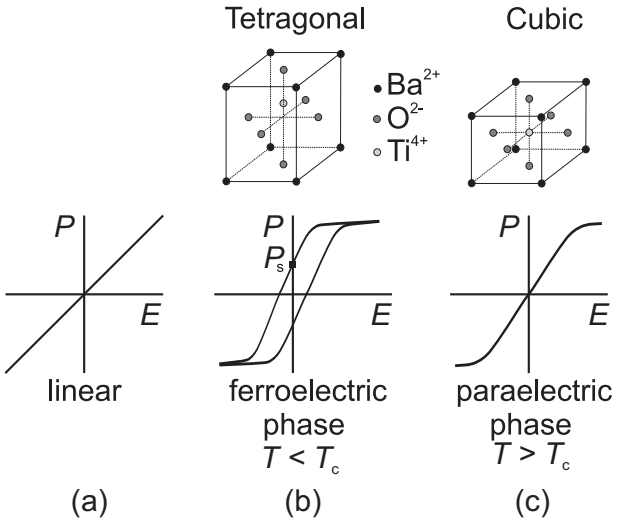


Figure 3.1 – In (a) the $P(E)$ response of a linear capacitor, in (b) a nonlinear capacitor in the ferroelectric phase (with hysteresis) and in (c) a nonlinear capacitor in the paralectric phase (without hysteresis).

Ferroelectric phase	**Paraelectric phase**
$T < T_c$	$T > T_c$
non-centrosymmetric	centrosymmetric
e.g., tetragonal crystal	cubic crystal
hysteresis	no hysteresis
spontaneous polarization P_s	no P_s
typically higher ε_r, η and $\tan\delta_\varepsilon$	typically high ε_r, and lower η and $\tan\delta_\varepsilon$

Table 3.1 – The ferroelectric and paraelectric phase of a ferroelectric material.

A *linear* capacitor has a constant ε_r, since the slope remains unaltered (see Figure 3.1a and also a measurement example in Figure 5.14). The ε_r of a *nonlinear* capacitor reduces with increasing $|E|$ due to the saturation of

the polarization (see, e.g., Figure 6.12). At the phase transition temperature of a nonlinear capacitor the crystal structure changes shape as depicted in Figure 3.1. The actual phase transition point, which affects the ε_r, is modeled by the Curie-Weiss relation for small-signals at $0\,V_\mathrm{dc}$ in the paraelectric phase

$$|\varepsilon_\mathrm{r}| = \frac{\varepsilon_0 C_\mathrm{curie}}{T - T_0} \tag{3.2}$$

with $\varepsilon_0 = 8.85{\cdot}10^{-12}\,\mathrm{F/m}$ the permittivity of free space, C_curie the Curie constant, and T_0 the Curie-Weiss phase transition temperature. T_0 is equal to or a few degrees Celsius less than the Curie temperature T_c [34].

In the ferroelectric phase, the capacitor exhibits a non-centrosymmetric crystal structure. For $BaTiO_3$ at room temperature it is a tetragonal distorted lattice. Dipoles in adjacent unit cells align and form domains, which are separated by domain walls [79].
The polarization without applying an (external) electric field is called spontaneous polarization P_s [79] and is due to a displacement of the ions from the cubic lattice positions (see Figure 3.1b). After the ferroelectric has been processed, the domains are randomly distributed and no residual polarization occurs [24].
Let's focus on a barium strontium titanate ferroelectric in the ferroelectric phase as an example (see the crystal structure in Figure 3.1). The titanium (Ti) is in the center of the octahedron, is shifted relative to the oxygen atoms in the ferroelectric phase and is relatively free to move in the octahedron [24]. When the Ti has moved from the center, a permanent dipole moment is formed, and the domains are formed in the ferroelectric [24].
A large external electric field changes the direction of the polarity and more domains will be aligned towards the direction of the electric field [24]. The ferroelectric phase induces a hysteretic $P(E)$ behavior which is dominated by the movement of domain walls [25]. Hysteresis correlates with an increase in dielectric loss (see Section 3.3) and a steeper $P(E)$ slope (compared to a capacitor in the paraelectric phase), which increases the $\varepsilon_\mathrm{r}(0\,V_\mathrm{dc})$, close to the coercive (switching) voltage, and hence C_max. The coercive field is defined as the electric field which is required to switch from P_s to zero P [34].
On the other hand, the paraelectric phase exhibits a centrosymmetric cubic crystal structure (see Figure 3.1c) without theoretically any spontaneous polarization nor hysteresis, resulting in a lower dielectric loss and ε_r.

When the polarization is fully saturated, the $\varepsilon_{r,min}$ will be similar in the ferroelectric and in the paraelectric phase, except for the $\varepsilon_{r,max}$, and consequently the tuning ratio increases with a higher $\varepsilon_{r,max}$ in the ferroelectric phase (see equation 3.6).

Single crystalline and poly-crystalline barium strontium titanate
Single crystalline ferroelectrics consist of a continuous lattice structure without any grain boundaries. The ε_r as a function of temperature of bulk single crystalline shows a peak of the ε_r at T_c which is extremely high in single crystalline materials due to a perfect dipole alignment, e.g., an ε_r of tens of thousands have been measured for $SrTiO_3$ [80]. Consequently, the $P(E)$ curve is very steep, and narrow attributing to a highly temperature-sensitive ε_r [81].
Poly-crystalline materials contain grain boundaries. The properties of poly-crystalline thin and thick films differ from those of single crystalline films [23, 25]. Typically, the transition between the ferroelectric and paraelectric phase is smeared out against the temperature due to local variations in stress, orientation, and additional defects such as grain boundaries [82–84], and compositional variations.

The single crystalline bulk value of $Ba_{0.7}Sr_{0.3}TiO_3$ at 300 K can reach an $\varepsilon_r = 5000$ [85]. The ε_r in thin poly-crystalline films is generally more than an order of magnitude lower (see Figure 6.17). Experimental results have shown that in thin films the relative permittivity ε_r, the tuning ratio η, and the phase transition temperature T_0 are lower, and the phase transition temperature region becomes wider compared to bulk ceramics [83, 86, 87].
A positive side-effect in thin films is that the ε_r is much less sensitive to temperature and these are therefore preferred in RF applications. A lower maximum ε_r compared to bulk materials is not important at high frequencies where capacitance values are typically small. The tuning ratio of thin films can already be sufficient for low-voltage applications.

The difference in ε_r between bulk ceramic and thin films can possibly be attributed to:

1) finer grains in thin films [82–84],

2) higher residual stress caused by thermal strain due to a difference in thermal expansion of the substrate and the ferroelectric during processing [83, 88, 89]. A CTE mismatch between the substrate and the

dielectric can lead to cracks, which form an electrical and mechanical reliability issue. For instance, crack can grow during thermal cycling and mechanical stress. The cracks are made visible by a microscopic inspection. To reduce the risk of cracks in the ferroelectric on silicon, the dielectric thickness should be sufficiently thin, and

3) a more pronounced influence of the low relative permittivity interface layer on the measured ε_r of thin films [87, 90]. The ferroelectric layer can in some cases be partly interfaced with an interface layer with a low relative permittivity, e.g., due to material diffusion through the electrodes. The effect of the passive interface layer on the device properties of a parallel plate capacitor near a single metal-ferroelectric interface is described in [23, 91] as

$$\frac{A}{C} = \frac{h}{\varepsilon_0 \varepsilon_\mathrm{r}} = \frac{h_\mathrm{film}}{\varepsilon_0 \varepsilon_\mathrm{film}} + \frac{h_\mathrm{interface}}{\varepsilon_0 \varepsilon_\mathrm{interface}} \tag{3.3}$$

with ε_r the measured relative permittivity, h the entire dielectric thickness, $\varepsilon_\mathrm{r,film}$ the relative permittivity of the ferroelectric, h_film the thickness of the ferroelectric film, $\varepsilon_\mathrm{r,interface}$ the relative permittivity of the passive interface layer and $h_\mathrm{interface}$ the thickness of the interface layer. The interface layer reduces the measured capacitance ($\varepsilon_\mathrm{interface} \ll \varepsilon_\mathrm{film}$) and therefore η. Hence, a capacitor with a thicker dielectric layer is less affected by an interface layer with a relative low $\varepsilon_\mathrm{interface}$ (see equation 3.3).

All three possible causes can contribute and depend on the deposition procedures.

Frequency response

A typical property of ferroelectric capacitors is that the measured capacitance decreases with increasing frequency because of dielectric relaxation, which causes a delay in polarization decreasing the relative permittivity linearly on a logarithmic frequency scale due to the Curie-von Schweidler time-behavior (see equations 2.13 and 2.14, and [37, 38, 92]). When properly measured and analyzed, resistive electrodes can also reduce the capacitance (see [36, 93] or paragraph 4.2.6). The capacitance decrease due to relaxation is small for BST [38] and therefore is not an issue for applications at RF.

3.2 Barium strontium titanate as a ferroelectric

The history of ferroelectrics goes back close to the beginning of the 20^{th} century. Pioneering research on ferroelectric properties in a crystal has been conducted by E. Schrödinger in 1912 [94] and J. Valasek in 1920 [95]. A profound scientific biography on Valesek and the discovery of ferroelectricity has been published in [96].

The term 'ferro-dielectric state' was introduced in 1935 by H. Mueller in his research on Rochelle salt [97] and 5 years later Mueller published an article in which he used the term 'ferroelectric temperature range' [98]. Since that year the term 'ferroelectrics' has been established.

The ferroelectric content in this work is based on solid-state poly-crystalline thin film barium strontium titanate ($Ba_xSr_{1-x}Ti_{1+y}O_{3+z}$; or in short BST). Over the years BST has shown promising material properties with respect to tuning ratio, dielectric loss, good temperature behavior, size and integration.
Since the 1940's numerous research groups worldwide have devoted research to $Ba_xSr_{1-x}Ti_{1+y}O_{3+z}$ [24, 32, 38, 40, 41, 48, 83, 99–106]. The understanding of the physical behavior of barium titanate ceramics started to evolve between 1940–1950 [24, 99]. Thin barium titanate films have been investigated since the 1960s [100].
Since the 1980s, barium strontium titanate has been developed amongst other complex ferroelectrics [107]. By mixing $BaTiO_3$ with $SrTiO_3$ a BST composition is created.
Bulk single crystalline $BaTiO_3$ has a $T_0 = 388\,\text{K}$ [108], is in the ferroelectric phase at room temperature, and has a high tuning ratio. Solid solutions of $BaTiO_3$ and $SrTiO_3$ shift the transition temperature close to room temperature to tailor the tuning ratio and loss.
In microwave applications low losses and low hysteretic effects are preferred. Therefore, for RF applications thin film ferroelectric capacitors in the paraelectric phase are often desired, in addition to the low temperature dependence. However, the capacitor should be optimized according to certain specifications depending on the application, since a trade-off exists between losses and tuning ratio (see [11, 109] or paragraph 2.2.2).
Since the mass production of handheld devices in the 1990s, the research on

ferroelectric components operating at microwave frequencies has been intensified and is still a lively research topic, as shown by the research groups studying the microwave performance of BST [40–42, 44, 45, 48, 73, 110, 111].

3.3 Figures of merit

In the literature the performance of ferroelectric capacitors operating at microwave frequencies is not unambiguously assessed by a single figure of merit. The most important first order performance parameters, during optimization, for ferroelectric BST capacitors at RF are the total quality factor [7]

$$Q = \frac{1}{\tan\delta} \tag{3.4}$$

with the total loss tangent $\tan\delta$. The $\tan\delta$ in this thesis is defined as the sum of the dielectric loss and the resistive loss. Losses cause a phase-shift δ of the voltage from the ideal 90° to the current. Detailed dielectric loss mechanisms of ferroelectric capacitors have been explained in [23, 41]. The intrinsic quality factor is expressed as

$$Q_{\text{intr}} = \frac{1}{\tan\delta_\varepsilon}, \tag{3.5}$$

with solely the dielectric loss $\tan\delta_\varepsilon$[1]. Note that, because of the use of both impedance and vector analyzer measurements, in Chapters 4 and 6, a distinction is made about the way the dissipation of the device (see equation 3.4) is indicated for impedance and vector analyzer measurements. A typical output of an impedance measurement of a capacitor is given by the capacitance and the $\tan\delta$. However, the output of a vector network analyzer measurement consists of S-parameters, which is converted to the quality factor (Q or Q_{intr}), since this is the most common parameter for circuit designers.

The tuning ratio is expressed as

[1] In this study, the extent of the dielectric loss is of more importance than the identification of the loss mechanisms, as discussed in [23, 41].

$$\eta = \frac{\varepsilon_{\mathrm{r}}(0\,V_{\mathrm{dc}})}{\varepsilon_{\mathrm{r}}(V_{\mathrm{dc}})} = \frac{\varepsilon_{\mathrm{r,max}}}{\varepsilon_{\mathrm{r,min}}} = \frac{C_{\mathrm{max}}}{C_{\mathrm{min}}}, \tag{3.6}$$

with the maximum capacitance C_{max} at $0\,V_{\mathrm{dc}}$ and the minimum capacitance C_{min} at the applied DC voltage (typically at the breakdown voltage), and the tunability

$$\text{tunability} = \frac{\varepsilon_{\mathrm{r}}(0\,V_{\mathrm{dc}}) - \varepsilon_{\mathrm{r}}(V_{\mathrm{dc}})}{\varepsilon_{\mathrm{r}}(0\,V_{\mathrm{dc}})} \cdot 100\,\% \tag{3.7}$$

To use the tuning ratio or tunability is a matter of taste.

The performance parameters are most often addressed separately as figures of merit or combined as shown by the commutation quality factor published by I.B. Vendik et al. [112]. The combined quality factor as in [112] is suited to compare the performance of applications like filters.

In this dissertation the equations of the Q, Q_{intr} and η are employed, since these are universally applicable to all applications of interest.

Chapter 4

Measurement methodology

4.1 Introduction

Ferroelectric materials can be electrically characterized by different test structures, measurement methodology, and measurement tools. The aim was to investigate the potential of ferroelectric capacitors for RF front-end applications. Therefore, measurements were limited to the low gigahertz range (typically up to 8 GHz). The most important first order parameters during optimization were addressed in Section 3.3. To assess these parameters the temperature-, frequency-, and electric field response need to be measured.

Measurements on test structures were performed at low and high frequencies. Impedance measurements have been performed on low frequency impedance analyzers up to 10 MHz. Measurements starting from hundreds of kilohertz (kHz) into the RF regime were performed on a Vector Network Analyzer (VNA).

This Chapter elaborates on the test structures, the equivalent capacitor model, the low-and high frequency measurements and methodology, the measurement hardware, and is finalized by a discussion and conclusions.

4.2 Top-patterned capacitor test structures

Fast processing and characterization cycles are desired for the material development of complex ferroelectrics used in high density planar capacitors. To study the material and electrical properties of thin barium strontium titanate films for low-voltage applications, a parallel plate metal-insulator-metal capacitor configuration was chosen, as the main device under test (DUT), to utilize for electrical characterization.

The alternative capacitor topology is an in-plane interdigital capacitor (IDC) configuration. IDC differ with respect to MIM capacitors [7] by their relatively large gap (typically $> 1\,\mu$m), large fringing capacitance, lower tuning ratio, and higher control voltages. For an IDC, a relative large part of the field lines travel through air compared to a MIM capacitor. The loss through air is negligible compared to the loss in the ferroelectric [113]. The processing of the IDC capacitors requires a single metal layer on top of the ferroelectric and a single lithography step.

A parallel plate MIM capacitor offers a high capacitance density at lower DC voltages, and a higher tuning ratio than an interdigital capacitor, since most of the electric field lines enter the ferroelectric, at the cost of a higher loss tangent [7]. The control voltage and power handling capability of a MIM capacitor can be easily manipulated by changing the dielectric thickness. Z. Ma et al. [114] showed that patterning of the top electrode only was also sufficient to perform electrical (1-port RF) characterization of MIM capacitors (see Figure 4.1).

4.2.1 Test structure description

The fundamentals of the MIM test structure, in this work, suited for 1-port RF measurements, as depicted in Figure 4.1, are based on the content of an article by Z. Ma et al. [114]. This test structure has become a common design to characterize ferroelectric capacitors (see, e.g., [115–117]).

A continuous metal bottom electrode acts as a virtual ground. The two outer probe pins of the GSG probe connected to ground were placed on the outer bondpad, and the signal-carrying pin was placed onto the inner metal surface of the circular DUT. RF test structures, suited for GSG impedance measurements, were measured using a single RF GSG probe. More detailed

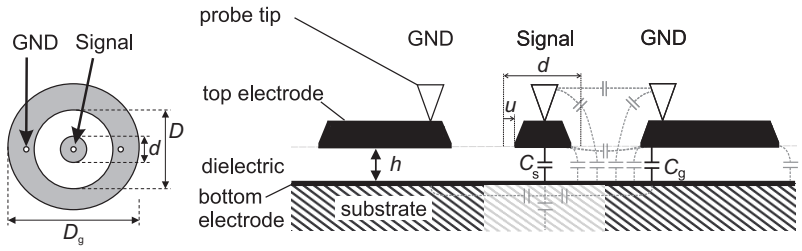


Figure 4.1 – On the left, a top view with 3 white (ground-signal-ground) probe landing spots in the middle, a gray signal pad in the center and an outer gray ground pad. On the right, a schematic cross section of a device under test to perform 1-port ground-signal-ground RF measurements. The bottom electrode and the dielectric layer are not patterned.

information on the measurement setup is addressed in Section 4.4.
When measuring the devices' capacitance, the probe measures a relatively large capacitance C_g of the large ground pad (diameter $D_g = 600\,\mu$m, with an opening $D = 100\,\mu$m) in series with a small capacitance C_s from the signal pad (diameter d) via the bottom electrode (see Figure 4.1).
The layout area has to be corrected for an undercut u of the top metal electrode and fringing fields. During isotropic etching, metal can be etched away underneath the photo resist. The layout area of the probe pads is thus reduced. An undercut is mainly important for smaller capacitor structures. The undercut leads to a change in device dimensions with $D_g - 2u$, $D + 2u$ and $d - 2u$.

4.2.2 The equivalent capacitor model

For the separation of the loss in the dielectric and the electrodes a series R-C model is best suited. The electrode resistance R_e is already in series (see Figure 2.3). The dielectric was modeled in Figure 2.3 as a parallel R_d-C_p combination, but it can be easily converted to the series R_d-C_s model of Figure 4.2:

$$R_d = R_p \frac{\tan^2 \delta_\varepsilon}{(1 + \tan^2 \delta_\varepsilon)} \tag{4.1}$$

and

$$C_s = C_p(1 + \tan^2 \delta_\varepsilon) \tag{4.2}$$

with

$$\tan\delta_\varepsilon = \frac{1}{Q_{\text{intr}}} = \omega R_{\text{d}} C_{\text{s}}. \tag{4.3}$$

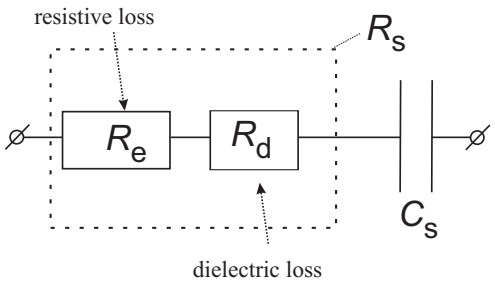


Figure 4.2 – The series R_s–C_s equivalent capacitor model. The loss tangent was typically determined at $0\,V_{\text{dc}}$ and a low V_{ac}.

C_s and R_s are determined from the measured S_{11}-parameters as follows. The complex impedance [118]

$$Z_{11} = Z_0 \frac{1+S_{11}}{1-S_{11}} \tag{4.4}$$

with the characteristic impedance $Z_0 = 50\,\Omega$ is then given by

$$Z_{11} = R_{\text{s}} + i\frac{-1}{\omega C_{\text{s}}} \quad \text{with} \quad R_{\text{s}} = R_{\text{e}} + R_{\text{d}}\,. \tag{4.5}$$

In Figure 4.2 the equivalent series resistance $R_s = \Re(Z_{11})$ at high frequencies, and the measured equivalent series capacitance can be approximated by

$$C_{\text{s}} \approx \frac{-1}{\omega\Im(Z_{11})}, \tag{4.6}$$

since $C_g \gg C_s$ (see Figure 4.1). The dielectric loss is denoted as $\tan\delta_\varepsilon$ and the electrode resistance is modeled by R_e (see equation 4.9).

4.2.3 Parasitic capacitances

Like all test structures, MIM capacitors contain parasitics. The parasitic capacitance contributions were determined by measurements, calculations, and simulations with the planar 3D full-wave electromagnetic simulation program Sonnet (version 11.53 [119]). The design of the test structures and the measurement data were used as an input for the Sonnet simulations.

The inner signal pad diameter d of the top electrode (see Figure 4.1) varies from $8\,\mu$m to $88\,\mu$m. Ferroelectric capacitors on a silicon wafer were measured to determine the dielectric layer thickness, ε_r, $\tan\delta$ and the parasitic resistances. These data were used further on for the Sonnet simulations. The parameters of the Ti/Pt (200 nm)/$Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ (110 nm)/Pt (100 nm)/Au (500 nm) MIM capacitors were characterized at 200 MHz ($0\,V_{dc}$). The measured relative permittivity was 170, the sheet resistance of the top electrodes $R_{s,t} \approx 70\,m\Omega/\square$, and the sheet resistance of the bottom electrode $R_{s,b} \approx 1.4\,\Omega/\square$. The parasitic capacitances of circular shaped capacitors with with signal pad diameters of $8\,\mu$m and $40\,\mu$m have been determined.

The dimensions, the shape and the undercut u of the capacitor were used to calculate the fringing fields using conformal mapping [113, 120]. Conformal mapping simply extends the area of the DUT to correct for fringing fields. The exact formula for the area extension [113] applied to the dimensions of the (typical) measured capacitive test structures, as depicted in Figure 4.1, including the undercut, results in an effective area of the inner signal pad

$$A_{eff} = \frac{1}{4}\pi d^2 + \pi d\left(\frac{2\ln(2)}{\pi}h - u\right) \tag{4.7}$$

The fraction in the right term of equation 4.7 between brackets takes into account the fringing fields. The undercut u was calculated by the slope of the (effective) capacitance density C/A_{eff} versus the ratio of the perimeter-effective area $\pi d/A_{eff}$ and was typically between $0.3\,\mu$m–$0.5\,\mu$m.

The main parasitics in Figure 4.1 are enlarged and indicated in Figure 4.3. All parasitic capacitances are identified and their contributions with respect to C_s are assessed for capacitors with a signal pad varying between $8\,\mu$m and $40\,\mu$m.

Equation 4.7 is employed to determine the parasitic fringing capacitance from the signal pad to the bottom electrode

$$C_1 = \varepsilon_0\varepsilon_r(\pi d)\left(\frac{2\ln(2)}{\pi}h - u\right) \tag{4.8}$$

As a results of fringing fields C_1/C_s (in %) for $d = 40\,\mu$m is 0.48 % and for $d = 8\,\mu$m is 2.43 %. C_1 as a result of fringing fields is incorporated in the effective area of the capacitor by conformal mapping. The parasitic

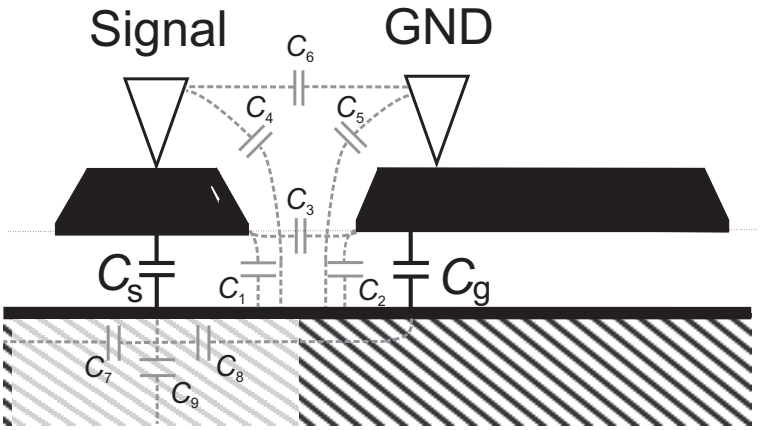


Figure 4.3 – A cross section of the RF device under test (DUT) (zoomed-in) with the identified parasitic capacitances C_1–C_9.

capacitance C_2 from the ground top electrode to the bottom electrode is negligible, because of the very large ground capacitance C_g. The capacitance from the signal pad to the ground pad through the dielectric C_3 can be neglected, since the distance between the contact pads is in the μm-range, while the dielectric thickness is in the nm-range, so that the electric field is screened by the bottom electrode. The parasitic capacitances C_4 and C_5 are removed by de-embedding using a calibration substrate. The capacitance C_9 from the middle of the bottom electrode of the DUT downwards into the 675 μm substrate has a very small ratio of the area of the (resistive) bottom electrode to the substrate thickness (at RF) and is estimated < 0.1 pF.

The parasitic capacitances C_6–C_8 were determined by Sonnet simulations. The capacitor stack in Sonnet is visualized in Figure 4.4.

The planar dielectric and metal layers were surrounded by grounded boxed walls and the capacitor electrodes were isolated from the grounded sidewalls, similar to the measurements. The GSG probe pins were simulated in a relatively simple way by three 4 μm $\times$ 4 μm lossless vias from the top boxwall to the top electrode of the signal and ground pad as depicted in the cross-section in Figure 4.4 and the topview in Figure 4.5.

The planar circular capacitive test structures were approximated by a regular octagon. The dielectric layers were modelled with material parameter

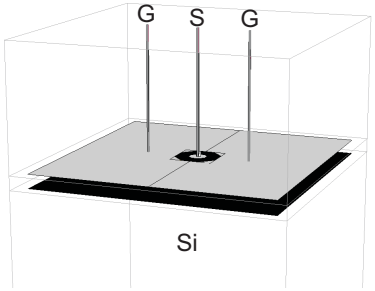


Figure 4.4 – A 3D image of the planar layers of a MIM capacitor test structure with vias as GSG probe tips inside a Sonnet design box.

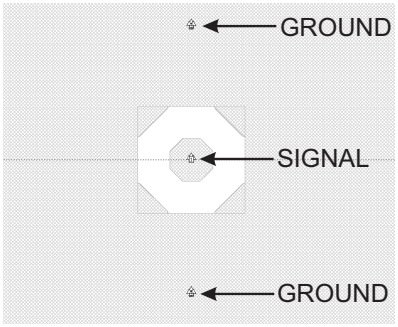


Figure 4.5 – A zoomed-in top view of a GSG MIM capacitor in Sonnet.

values as given in Table 4.1 with the relative permittivity ε_r, the relative magnetic permeability μ_r and the dielectric conductivity σ. These values are constant and were chosen to match the measured values at 200 MHz and $0\,V_{dc}$. The resistive electrode layers were adjusted according to the measured sheet resistances of the electrodes.

Layers	Thickness h	ε_r	μ_r	$\tan\delta_\varepsilon$	σ
air	1 μm	1 or $1{\cdot}10^{-4}$	1 or $1{\cdot}10^{-4}$	0 %	0 S/m
BST	0.11 μm	170	1	1 %	0 S/m
Si	675 μm	11.9	1	0.04 %	5 S/m

Table 4.1 – Layer properties of the dielectric layers in Sonnet.

The parasitic inductance of the vias was neglected in Sonnet by setting μ_r to $1{\times}10^{-4}$. The parasitic capacitance C_6 between the ground and signal probes and pads was simulated, by setting the relative permittivity of air to $1{\times}10^{-4}$, then to 1 and finally comparing the simulated equivalent series capacitance. The results showed that capacitance C_6 was in the low fF-range and is hence negligible compared to a capacitor with a $d \geq 8\,\mu$m (see also the ε_r and h for a BST MIM capacitor in Table 4.1). Therefore there was no need for separate calibration or de-embedding structures at the cost of neglecting a part of the device capacitance and inductance. The capacitance C_8 parallel to the bottom electrode through the silicon substrate was determined by performing Sonnet simulations without a bottom electrode. Less than 20 fF was obtained for a capacitor with an inner diameter of 40 μm.

A small physical area of a thin film ferroelectric capacitor can already result

in a relatively large measured capacitance (see the capacitance density in Table 6.4). The parasitic capacitances were identified, partly calculated and simulated in Sonnet. The influence of all parasitic capacitances, compared to the measured capacitance, differ individually more than a factor of 100, and were neglected.

4.2.4 Parasitic resistances

The parasitic resistances in our DUT are directly related to the top and bottom electrode. Utilizing the measured equivalent capacitor model in Figure 4.2, the measured loss tangent in equation 3.4 can now be written as

$$\tan\delta \;=\; \frac{1}{Q} \;=\; \frac{\Re(Z_{11})}{|\Im(Z_{11})|} \;=\; \tan\delta_{\varepsilon} \;+\; \omega C_{\mathrm{s}} R_{\mathrm{e}} \tag{4.9}$$

The latter term $\omega C_{\mathrm{s}} R_{\mathrm{e}}$ represents the resistive electrode loss. The geometry of the electrodes determines the resistance R_{e} [114, 121].
R_{e} is modeled in order to separate the measured dielectric loss (see also equation 3.5) from the measured resistive loss at zero DC bias. In the lumped element case R_{e} is approximated by the sum of the resistance of the center (signal) pad (see Figure 4.1 and 4.6)

$$R_{\mathrm{center}} = \frac{R_{\mathrm{s,t}} + R_{\mathrm{s,b}}}{8\pi}, \tag{4.10}$$

and the resistance of the bottom electrode between the signal and ground pad is expressed as

$$R_{\mathrm{ring}} = \frac{R_{\mathrm{s,b}}}{2\pi} \ln\left(\frac{D}{d}\right) \tag{4.11}$$

The resistance R_{outer} equals the resistance of the bottom electrode below the ground probes. A schematic circuit is depicted in Figure 4.6. Any lumped capacitor becomes a distributed equivalent network at high enough frequencies. This will be discussed in paragraph 4.2.6.

R_{outer} was neglected because of the larger diameter $D \gg d$ (see Figure 4.1). The contact resistance of the electrodes at the probe tip was measured on

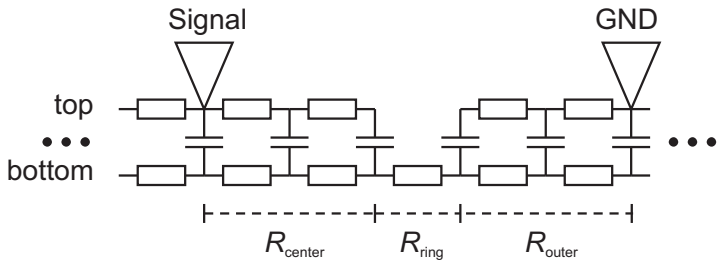


Figure 4.6 – Any lumped capacitor becomes a distributed *R-C* chain at high enough RF. The capacitances corresponding to the electrical fields through air and substrate (not drawn) are still negligibly small with respect to the large capacitances of the MIM capacitor.

an unpatterned top electrode with $R_{\mathrm{short,top}} \approx 0.1\,\Omega$ and is hence negligible. This results in a resistance

$$R \approx \vartheta R_{\mathrm{s,b}} \quad \text{with} \quad \vartheta = \frac{1}{2\pi}\left(\frac{1+\nu}{4} + \ln\frac{D}{d}\right), \tag{4.12}$$

$$\text{and} \quad \nu = \frac{R_{\mathrm{s,t}}}{R_{\mathrm{s,b}}} \quad ,$$

described by the product of the sheet resistance $R_{\mathrm{s,b}}$ of the bottom electrode and an electrode geometry factor ϑ. The sheet resistance ratio ν is negligibly small for well conducting top electrodes, e.g., $R_{\mathrm{s,t}} = 70\,\mathrm{m\Omega}$ and $R_{\mathrm{s,b}} = 1.4\,\Omega$ (see the heading on parasitics in subsection 4.2.3), which gives $\nu = 0.05$.

By applying equation 4.12, the dielectric loss can be separated from the resistive loss, as described in the upcoming paragraph, in which the RF measurement technique is discussed.

4.2.5 Loss tangent separation technique

The loss tangent is the sum of the dielectric loss and the resistive electrode loss. To determine both loss contributions a separation technique was proposed [36], which uses at least three circular shaped test structures with different inner diameters. No additional de-embedding structures are required.
In Figure 4.7 the loss tangent is plotted against the product of the measured series equivalent capacitance C_{s} and the the calculated geometry factor ϑ.

The slope of the curves is equal to $\omega R_{\mathrm{s,b}}$, as expressed in equations 4.9 and 4.12. The dielectric loss tangent $\tan\delta_\varepsilon$ is determined by a linear extrapolation to the intercept point at $\tan\delta(C_\mathrm{s}\vartheta)$ in Figure 4.7 at $f = 8\,\mathrm{GHz}$ and is slightly frequency dependent.
A deviation from the linear line at small radii would suggest an influence of the edges of the capacitors, e.g., by damage during processing caused by reactive ion etching, increasing the loss tangent. A deviation from linearity at large radii suggests strong distributed effects, which decrease the capacitance and increase the loss tangent.

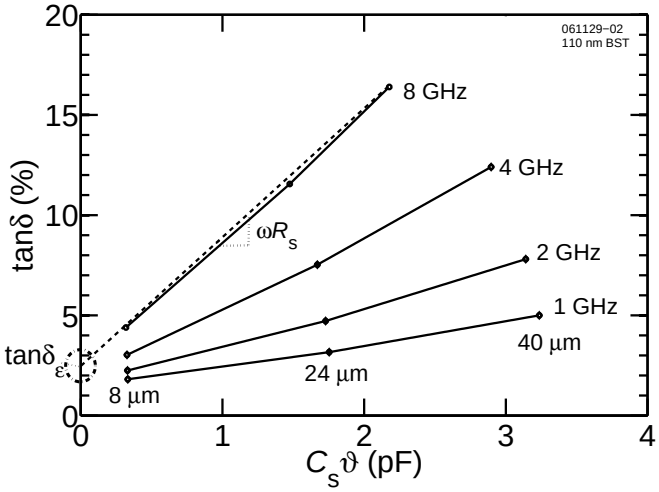


Figure 4.7 – The measured dielectric and the resistive loss tangent are separated using a linear regression of a $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ MIM capacitor.

The (total) loss tangent of test structures with an inner diameter of 40, 24 and 8 μm is shown. A smaller inner diameter decreases the $\tan\delta$ at RF.

Employing the same way of showing the data in Sonnet, the distributed effects for physically large capacitors becomes clearly visible as depicted in Figure 4.8.

The Sonnet simulation results (see Figure 4.8) show a close resemblance to the measured capacitors with a diameter smaller than 40 μm (see Figure 4.7). For $d \geq 40\,\mu\mathrm{m}$, the inductance of the short and load calibration standards notably reduce C_s, increase the $\Im(Z_{11})$ and therefore reduce $\tan\delta$.

To calculate the $\tan\delta_\varepsilon$ the measured total loss is extrapolated to $C_\mathrm{s}\vartheta \to 0$

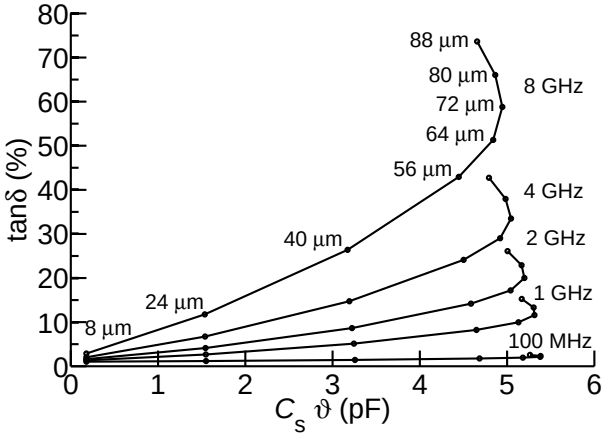


Figure 4.8 – Sonnet simulations showing the influence of distributed effects at multiple frequencies on capacitors with a relatively large inner diameter.

for each frequency using all data from $d = 40$ to $8\,\mu$m and $d = 24$ to $8\,\mu$m. In Figure 4.9 the measured $\tan\delta_\varepsilon$ and the resistive loss are separated across the entire frequency span.

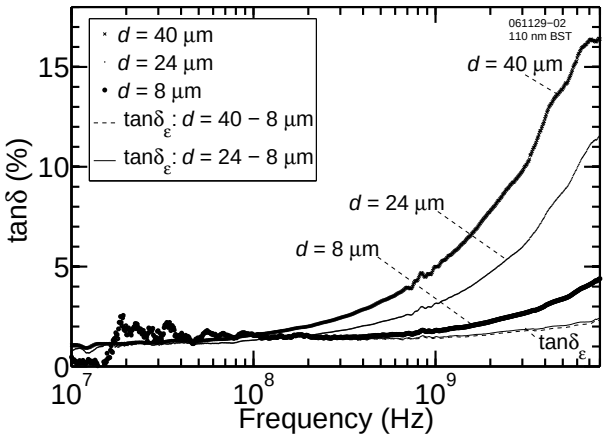


Figure 4.9 – The measured losses with and without subtraction of the resistive bottom electrode losses on Si.

A graphical outline of the measurement data of more than two capacitors in Figure 4.9 can be used to easily separate the dielectric loss from the resistive electrode loss, as expressed in equation 4.9. It is especially suited to determine the frequency dependence of the dielectric loss tangent $\tan\delta_\varepsilon$.

The results in Figure 4.9 show a typical ferroelectric behavior of increasing dielectric losses with increasing frequency.

4.2.6 Distributed effects

A property of ferroelectric capacitors is that the measured capacitance decreases with the frequency due to dielectric relaxation (see Chapter 3). However, distributed effects also can play a role [93]. A lumped capacitor becomes distributed at a high enough frequency due to the resistivity of the electrodes (see also Figure 4.6). At RF, the resistance-capacitance chain leads to a voltage drop at the edges of the capacitor, because of lateral electrode connections, which will act as if the area of C_s is reduced. A reduced R_center is accompanied by a reduced C_s (deviation from the logarithmic decline in capacitance in Figure 4.10).

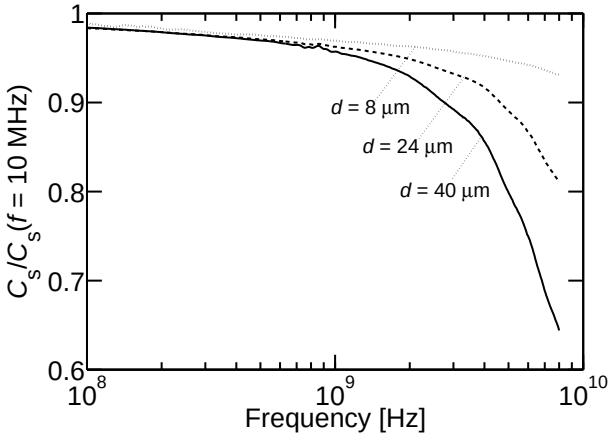


Figure 4.10 – The measured normalized capacitance at 10 MHz declines due to relaxation effects. Above $f = 400$ MHz the distributed nature of the capacitor reduces the capacitance severely, especially for large capacitors.

The diameter of the DUT is important. A larger area results in a higher capacitance, a lower $\Im(Z_{11})$, and a higher $\tan\delta$ (see equation 4.9 and Figure 4.7). The decrease of the capacitance due to relaxation effects is independent of the signal pad diameter, and is relatively small, compared to the much stronger decrease due to distributed effects from a few hundred megahertz onwards (see Figure 4.10).

To confirm that distributed effects cause the severe decrease in relative permittivity for large capacitors at high frequencies, simulations were performed in the planar 3D full-wave electromagnetic simulation program Sonnet [119].
The capacitor stack was simulated with lossless and lossy electrodes with Sonnet (see paragraph 4.2.3). The one-port response of the simulated C_s and $\tan\delta$ at different frequency points are depicted in Figure 4.11.

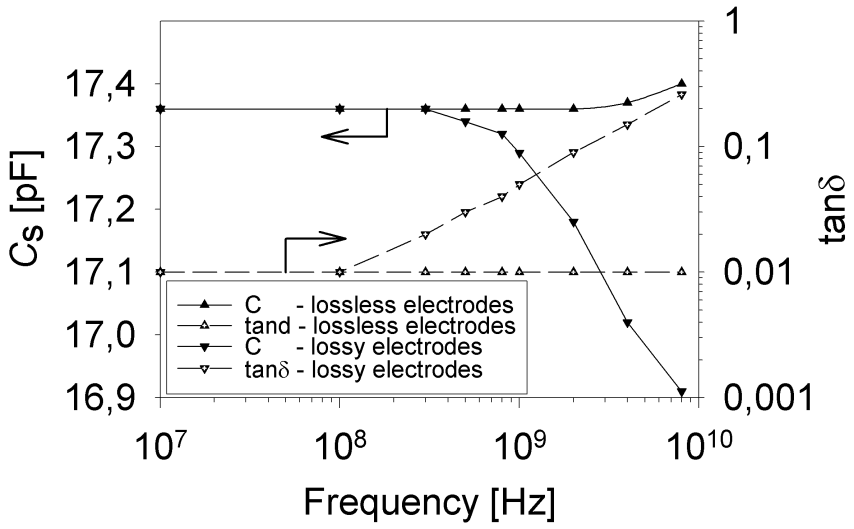


Figure 4.11 – Planar electromagnetic simulations in Sonnet [119] show the capacitance of a test structure with a signal pad diameter of 40 μm with lossless and lossy electrodes. No relaxation effects were included in the simulations. At high frequencies, the sheet resistance of the electrodes determines mainly the capacitance roll-off and the increase in $\tan\delta$.

The strong frequency dependent influence of the resistive electrodes on the C_s and $\tan\delta$ is confirmed. The electrode resistance and the capacitance density determine the extent of the distributed effects (see Figure 4.2), i.e., if the capacitance density in one sample is higher than in the other, the $\Im(Z_{11})$ will be lower, and if $\omega C_\mathrm{s} R_\mathrm{e} > \tan\delta_\epsilon$, and consequently $\tan\delta$ will increase due to the dominant resistive losses at high frequencies.

To substantiate the importance of the electrodes at RF three samples were realized with Pt electrodes, and with a Pt/Au (top) and Pt/Au/Pt (bottom) electrode configuration. The series resistance of the electrodes was determined from the constant value of $\Re(Z_{11})$ at high frequencies, e.g, 8 GHz.

The decrease of the measured frequency response of $\Re(Z_{11})$ is depicted in Figure 4.12, and shows the effect of the conductivity of the electrodes.

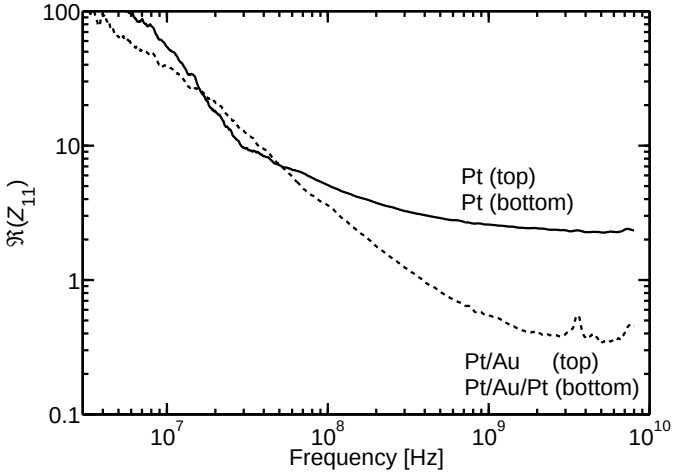


Figure 4.12 – $\Re(Z_{11})$ measurement results against frequency for $30\,\mu\text{m} \times 30\,\mu\text{m}$ ferroelectric MIM capacitors on two samples with a $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ layer sandwiched in between 1) Pt electrodes, and 2) a Pt (100 nm)/Au (500 nm) top electrode and Pt (200 nm)/Au (500 nm)/Pt (50 nm) bottom electrode.

The series resistance, which partially contains the contact resistance of the wafer probes, drops from $2\,\Omega$ (Pt/(BST)/Pt stack) to $0.4\,\Omega$ (Pt/Au/Pt/(BST)/Pt/Au stack) at 8 GHz. The impact on the $\tan\delta$ is depicted in Figure 4.13 by the ratio of the sample with solely Pt electrode and the sample with the Pt/Au/Pt-$Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$-Pt/Au stack.

The $\tan\delta$ was relatively constant with the frequency up to the low MHz frequency range for BST capacitors with an area of $30\,\mu\text{m} \times 30\,\mu\text{m}$. The $\tan\delta$ at 1 GHz decreases with a factor of 4 for better conducting electrodes. The simulated and measurement results stipulate the importance of good conducting electrodes to reduce the measured loss tangent at RF, which corresponds with results in literature [7]. The effect on the tuning ratio will be discussed in paragraph 6.5.4.

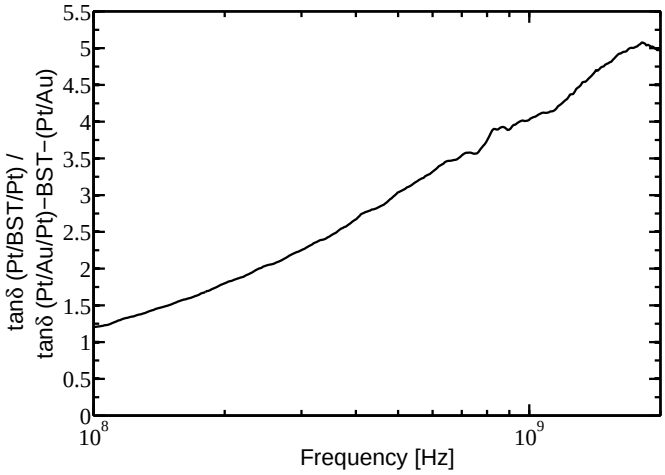


Figure 4.13 – The loss tangent of 30 μm × 30 μm ferroelectric capacitors on two samples with a $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ layer sandwiched in between 1) Pt electrodes, and 2) a Pt (100 nm)/Au (500 nm) top electrode and Pt (200 nm)/Au (500 nm)/Pt (50 nm) bottom electrode.

4.3 Low frequency measurement methodology

At low frequencies (LF), the frequency-, voltage-, and temperature dependence of ferroelectric capacitors were studied. To this purpose, impedance measurements were typically performed at low frequencies from 100 Hz–10 MHz. During the frequency sweep, the AC and DC voltages were superimposed in the impedance measurement hardware.
The characterization with the LF measurement equipment is accurate for wide-band frequency measurements due to an internal auto-balancing bridge. Four terminal pair cabling is used (high and low potential, and high and low current). Different range resistors have been implemented in the internal measurement circuit necessary for measuring an impedance. A detailed description of the functioning of an auto-balancing circuit is given in [122]. A wide-band impedance accuracy of typically 0.1 % is achieved up to 40 MHz through auto-balancing of the circuit [123].

The LF measurements were performed with both a signal-carrying probe and ground probe. On the outer part of the wafer a large part of the top

metal was left unpatterned. The signal-carrying probe was placed onto this large outer part and therefore most likely a short exists to the bottom electrode. The probe connected to ground was placed on the signal pad of the test structure. Thus, the signal-pad electrode is in connection with ground and the bottom electrode in connection with the signal-carrying probe.

4.3.1 Frequency and voltage sweeps

At low frequencies, wide-band measurements of the ferroelectric capacitors were performed with a parallel capacitance and a parallel resistance circuit mode on the analyzer. MIM capacitors were measured with typical signal pad dimensions of $100\,\mu\mathrm{m}\times 100\,\mu\mathrm{m}$, or $250\,\mu\mathrm{m}\times 250\,\mu\mathrm{m}$.

An HP4194a impedance analyzer was used, up to 10 MHz, to obtain the relative permittivity ε_r and the loss tangent $\tan\delta$ at $50\,\mathrm{m}V_\mathrm{ac}$. Pre-programmed automatic and continuous voltage sweeps could be performed up to $40\,V_\mathrm{dc}$. Automated impedance measurements were carried out using a PI Physik Instrumente C-560 stepping motor controller, a Keithley 708 switching system, a probe card, and a HP4284a precision LCR meter (see Figure 4.14).

Figure 4.14 – Automated impedance measurement setup with 1) a HP4284a precision LCR meter, 2) a Keithley 708 switching system, 3) PI Physik Instrumente C-560 stepping motor controller, 4) wafer chuck and probe card, and 5) Sefelec PM04 milliohmmeter.

In Figure 4.14, a second Keithley 708 switching system is connected with the aforementioned LCR meter, and a Sefelec PM04 milliohmmeter, to manually measure the sheet resistance of the top electrode of the MIM capacitor using 4 probes. The corresponding schematic is shown in Figure 4.15.

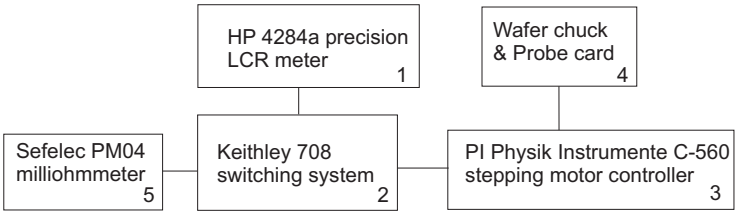


Figure 4.15 – The schematic of the automated impedance measurement setup.

4.3.2 Temperature sweeps

Temperature measurements were performed using the measurement setup as depicted in Figure 4.16. The setup consists of a Novocontrol Quatro

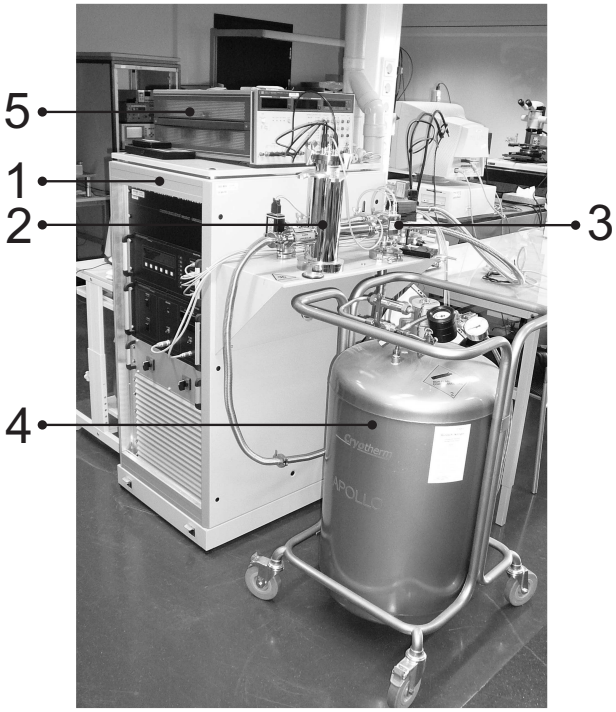


Figure 4.16 – The cryostat measurement setup for temperature measurements from -160 °C up to 300 °C using 1) a Novocontrol Quatro cryostat, 2) a BDS1100 sample holder, 3) a Novocontrol BDS1330 heating controller, 4) a liquid nitrogen tank, and 5) an HP4192 Impedance Analyzer.

cryostat, a BDS1100 sample holder, a Novocontrol BDS1330 heating controller, a liquid nitrogen tank, and an HP4192 Impedance Analyzer.

The cryostat enables a temperature as low as -160 °C up to 300 °C. The sample holder can only carry a single sample. Samples were glued on a copper substrate with a silver solution. A portion of the silver solution was deposited on top which is in connection with the bottom electrode. The signal pad of a test structure with a top electrode area of about 275.000 μm^2 was vertically probed. A Novocontrol BDS1330 heating controller was employed to heat the sample above ambient temperature, and a liquid nitrogen tank was used for cooling down. The frequency, AC voltage and DC voltage were applied with the impedance analyzer.
Typically, the measurements took place at zero DC bias and an AC voltage of 0.1 V_{ac}. A measurement frequency of 100 kHz is chosen, since it is low enough to avoid electrode and contact resistance influence, which would increase $\tan\delta$. In addition, this measurement frequency is sufficiently high to perform accurate capacitance measurements, since at low frequencies the impedance of the small capacitors becomes very high.

4.4 High frequency Vector Network Analyzer methodology

To electrically characterize GSG 1-port test structures an Advantest R3767CG vector network analyzer (VNA) was employed that supports wideband measurements from 300 kHz up to 8 GHz (see Figure 4.17). A VNA generates AC signals, and can record the magnitude and phase of the reflected and transmitted signals. 1-port VNA measurements record the S_{11} reflection parameters, which can be transformed to Z_{11} impedance parameters to extract the ε_r, $\Re(Z_{11})$, Q, and C_s (see Section 4.2.2 and equation 4.9). The measurements were limited to small-signals typically at -10 dBm.

RF capacitance-voltage measurements require a bias-tee to be connected to the measurement port of the VNA (see Figure 4.17).

The DC bias voltage of the device under test is supplied by a Keithley 237 high-voltage source. The AC signal, from the VNA, is added to the DC voltage using a bias tee. (Bias tees are further explained in the next Chapter.) The signal reaches the DUT, which is placed on a very thick alumina chuck isolator, through a 125 μm pitch GSG probe and the AC signal partly reflects back, through the bias tee, to the VNA, where amplitude and phase are measured.

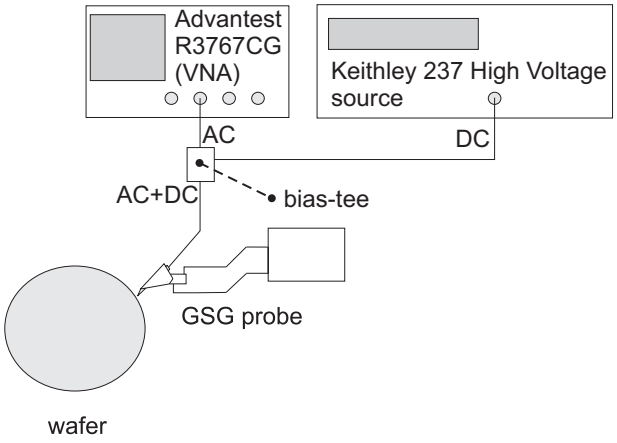


Figure 4.17 – A schematic of a 1-port RF measurement setup with a GSG probe.

The radio frequency response of the test structures were typically measured at small-signals with an RF power of -10 dBm, at ambient temperature.

Before performing any device measurement with any VNA, a calibration is required to quantify the parasitic capacitance, inductance and resistance of the measurement hardware.
Measurement uncertainty affects the measured capacitance as described in [121, 124]. 1-port RF characterization of the devices presented in Section 4.2.1 requires a short-open-load calibration. Short and load calibration standards are not ideal standards. They also contain parasitic inductances, which add up to the impedance of the standards. This will cause inaccuracies in the measurement data, if the user-defined calibration kit within the VNA is not adjusted properly, or if no correction factor is taken along in the parameter extraction program. In our case no quantified correction terms by the calibration kit manufacturer are known, since our probe dissents from the advised one. An additional inductance caused by an incomplete impedance compensation of the short and load standard affects the measured capacitance with frequency. A manual correction by including an inductance L to the impedance parameters changes the reactive part of the impedance and therefore the capacitance value changes as depicted in Figure 4.18.

In our case the VNA assumes zero inductance for the combination of the GSG probe and the short or load measurement. Typical inductances for the used probes are between 2 nH–10 nH [125]. When the missing inductance is

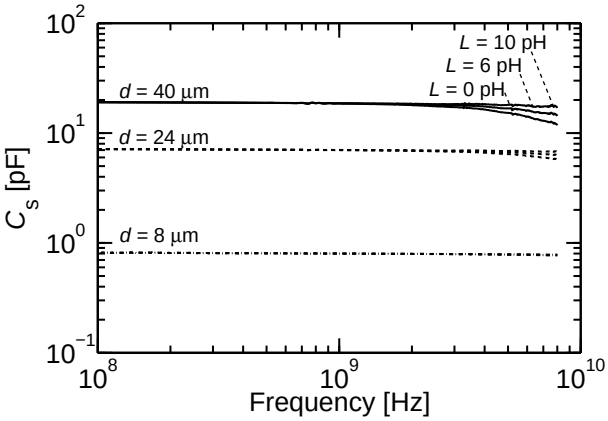


Figure 4.18 – The effect of an additional inductance of $L = 0$, 6 and 10 pH on the measured equivalent capacitance with frequency for devices under test with an inner diameter of $d = 40$, 24, and 8 μm.

added the measured impedance becomes

$$Z_{11} = R_{\mathrm{s}} - \frac{i}{\omega C_{\mathrm{s},L=0}} + i\omega L, \quad \text{with } C_{\mathrm{s},L=0} = \frac{-1}{\omega \Im(Z_{11})}. \tag{4.13}$$

All measurements on alumina and Si were performed without additional inductance correction programmed in the VNA or without a post-inductance correction factor by Matlab S_{11}-parameter analysis software.

4.5 Discussion and conclusions

MIM test structures were designed that enable fast characterization cycles of ferroelectric layers. Parasitics can significantly affect the measured capacitance, e.g., due to the measurement setup as indicated in [126]. However, in Section 4.2.3 it has been argued that the parasitic capacitance contributions in our MIM capacitors can be neglected, since the measured capacitance of the thin film (high capacitance density; see Table 6.4) ferroelectric capacitors is relatively large compared to the parasitic capacitances.

Besides parasitic capacitances also parasitic resistive contributions can affect the measurement capacitance. With increasing frequency the lumped series capacitor C_{s} becomes a distributed resistance-capacitance network (see paragraph 4.2.6). Distributed effects start to play a role when the

imaginary part of the impedance is relatively low compared to the real part, e.g., by a relatively high capacitance value at high frequencies. The geometry of the capacitor determines the significance of the distributed effects. When distributed effects are present, measurements will show that the capacitance severely reduces and that the loss tangent increases with the frequency. This was shown by plotting the $\tan\delta$ (see equation 4.9) against $C_s\vartheta$ (see Figure 4.7). Typically capacitors with a signal pad diameter below $40\,\mu$m were tested, to avoid coming into the distributed regime.
A loss separation technique is proposed (see Section 4.2.5), which can separate the resistive loss from the dielectric loss, by measuring three different relatively small capacitors ($d \leq 40\,\mu$m).
Furthermore, this technique can: 1) correct for the measured inductance ($L = 0$–$10\,$pH; see paragraph 4.4) as a results of the short and load calibration standards, by plotting against C_s, 2) possibly indicate process-induced damage of small radii signal pad GSG capacitors by showing an increase in loss tangent, and 3) show pronounced distributed effects for large signal pad radii.

This wide-band characterization technique contributes to the insight in the quality of the dielectric and the resistive loss contribution. Using this knowledge the process flow should be adapted during optimization, e.g., by changing the dielectric composition, decreasing the sheet resistance of the electrodes, etc.

Chapter 5

Wide-band bias-tees for capacitor characterization

5.1 Introduction

A bias-tee is required to perform RF $C(V_{\mathrm{dc}})$ measurements. The function of a three-port bias-tee is to superimpose a DC input voltage with an AC signal [127]. Many impedance analyzers have built-in bias networks, but most require external bias-tees for high voltages (typically above $40\,V_{\mathrm{dc}}$). *High-voltage* wide-band bias-tees are commercially available for frequency ranges from the kHz-range to the GHz-range. These are well suited for many types of measurements such as short pulse measurements. We want to tune the ferroelectric capacitors using a DC bias and to simultaneously measure the impedance across a wide frequency span with a small AC signal.

The desired requirements of the bias-tee are specific to measure thin film ferroelectric capacitors:

- The frequency sweep should start from 300 kHz to 8 GHz, which are the minimum and maximum frequencies of our VNA.
- from 0–$100\,V_{\mathrm{dc}}$. This is more than sufficient for our thin film capacitors.
- it should protect the VNA against voltage spikes.

A commercial, very wide-band (f = 20 kHz–18 GHz), high-voltage (max. 200 V) Picosecond 5530A-104 bias-tee [128], suited for low-current applications, was utilized.
During the RF $C(V_{\mathrm{dc}})$ measurements, voltage-dependent impedance measurements errors occurred slightly below 3 MHz and a resonance occurred at 3 MHz, even without measuring a device under test.

In this Chapter, after the background knowledge on bias-tees in section 5.2, the observed measurement errors are discussed in more detail in section 5.4, and two approaches are presented on how to circumvent these errors. This chapter will end with a discussion and conclusions.

5.2 Background knowledge on bias-tees

Bias-tees are electronic circuits that supply a DC voltage to a DUT, while the AC measurement signal can propagate undisturbed from the measurement equipment to the DUT and back. A series coupling capacitor C_{bt} between the AC ports (see Figure 5.1) blocks the DC signal from the measurement equipment connected to port 1. A resistor R_{bt} and/or a coil L_{bt} provide a DC current and voltage to the device at port 3, while blocking the AC signal from the DC power supply connected to port 2.

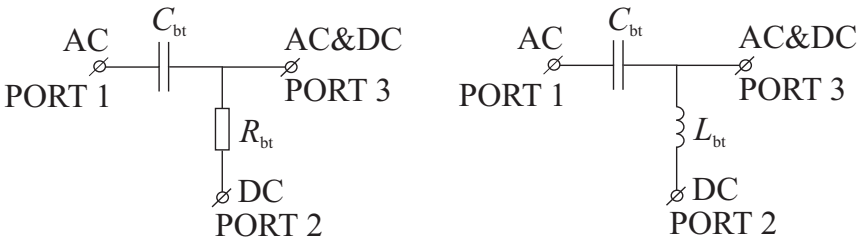


Figure 5.1 – Simple and commonly bias-tee designs with an *R-C* or an *L-C* architecture.

The choice between a resistor and an inductor depends on the amount of DC current required for the application. For relatively small currents a resistor is used, while for relatively large currents, e.g., $I > 10$ mA, inductors are used. Inductors likely become self-resonant at higher frequencies due to parasitic capacitances and a multi-stage design is required to suppress those resonances. Resistors can provide a flat impedance over a wide frequency

range and are preferred, if the small AC dissipation and the DC current limitation can be accepted.

Wide-band bias-tees need high value coupling capacitors C_{bt}. The impedance of the coupling capacitor should fulfill the relation

$$Z_{\mathrm{C}} = R_{\mathrm{e}} + \frac{i}{\omega_{\mathrm{c}} C_{\mathrm{bt}}} \tag{5.1}$$

and the impedance must be sufficiently low:

$$|Z_{\mathrm{C}}| \approx \frac{1}{\omega_{\mathrm{c}} C_{\mathrm{bt}}} \lesssim 50\,\Omega \tag{5.2}$$

at the lower cut-off frequency ω_{c}. The coupling capacitor will otherwise reflect most of the AC signal. The series resistance R_{e} models the power dissipation of C. The resistance of the capacitance R_{e} is approximately equal to the resistance of the metallic electrodes and connectors. The coupling capacitors should be small in physical size to avoid parasitic inductances and resonances at high frequencies.

5.3 Commercial bias-tees

Many commercial high-voltage wide-band bias-tees utilize ferroelectric coupling capacitors, which are much smaller in physical size compared to voltage-independent (type NP0) capacitors with the same voltage rating. Albeit, this comes at the expense of a substantial voltage-dependence.
The influence of a variable coupling capacitor is strongest at low frequencies when the imaginary part $(\omega_{\mathrm{c}} C_{\mathrm{bt}})^{-1}$ becomes a significant fraction of the impedance of the DUT. At high frequencies the impedance of a ferroelectric (coupling) capacitor (see equation 5.1) is dominated by the series resistance of the metal electrode layers $Z_{\mathrm{C}} \approx R_{\mathrm{e}}$. The voltage-independence of the series resistance of the metal electrodes, thus allows for a voltage-independent calibration at high frequencies.

The next section discusses the properties of ferroelectric capacitors in more detail and two approaches to reduce measurement errors during a wide-band characterization of ferroelectric capacitor devices.

5.4 Wide-band ferroelectric capacitor characterization

Determining the first order performance parameters, e.g., ε_r and $\tan\delta$, of the capacitive test structures in the kHz–MHz frequency range is crucial for obtaining insight into the quality of the dielectric layers. In the kHz-GHz frequency range, the measurement errors caused by a bias-tee with an applied DC bias, should preferably be negligible during the characterization.

Two options were brought up to reduce the measurement errors caused by a voltage-dependent commercial bias-tee at low frequencies and are addressed in paragraphs 5.4.1 and 5.4.2.

5.4.1 Reducing voltage dependence by calibration

To investigate a DC-voltage dependence of a commercial bias-tee, a simple experiment was designed utilizing two of these bias-tees back-to-back. The experiment is shown in Figure 5.2. The transmission of the signal travels from port P1 to port P2, through these two bias-tees, and should not depend on the applied DC biases on either of the bias-tee. Non-idealities in the bias-tee might lead to a bias-dependent phase shift or attenuation, either of which is easily measured from port P2.

To demonstrate the effect of a voltage stress on the transmission path, the phase of the signal was analyzed. The phase error determines the accuracy of capacitance measurements. In the experiments an Advantest R3767CG VNA was used with external bias-tees. A commercial, very wide-band (f = 20 kHz–18 GHz), high-voltage (max. 200 V) Picosecond 5530A-104 bias-tee [128], suited for low-current applications, was utilized. A two-port measurement setup was used and two Picosecond bias-tees were connected in series, so that the AC ports are connected to the ports of the VNA (see Figure 5.2).

The DC voltage was isolated from the VNA by the blocking capacitor in each bias-tee. The phase of the transmission signal S_{21} was analyzed. After a short-open-load-through (SOLT) calibration (at V_{dc} = 0 V) the bias-tees were measured at V_{dc} = 0 V and disconnected. The bias-tees were then terminated with a short or a load SMA connector, after which, temporarily, a $V_{dc} = 60$ V voltage-stress was applied on one of the DC voltage ports.

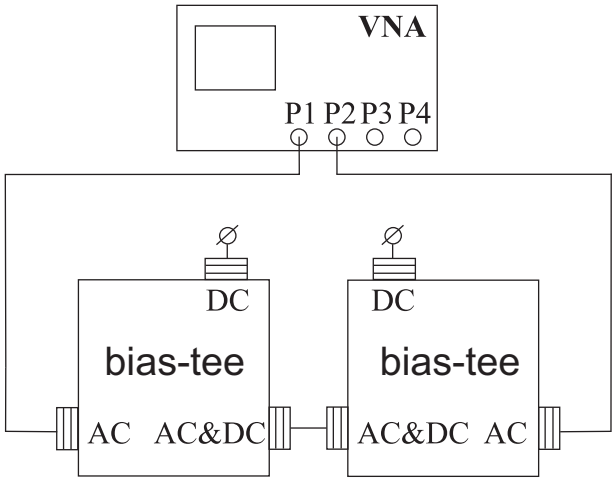


Figure 5.2 – The RF measurement setup for determining the phase difference over frequency before and after applying $V_{\mathrm{dc}} = 60$ V. Two commercial bias-tees Picosecond 5530A-104 were connected in series to port 1 (P1) and 2 (P2) of the VNA. The AC power of the VNA was set at $P_{\mathrm{AC}} = 0$ dBm.

Then the bias-tees were connected again to the RF measurement setup and the S-parameters were obtained (without DC voltage). The phase of the transmission S_{21} before the voltage stress was subtracted from the phase after stress and the outcome is depicted in Figure 5.3.
The effect of a DC voltage stress on the bias-tee is evident. The change in phase can be explained by two causes:

1. a *remanent* change in coupling capacitance C_{bt}, integrated in the bias-tee, causes the smooth phase increase at low frequencies. Ferroelectric (coupling) capacitors exhibit this behavior, are non-linear and exhibit hysteresis.

2. a resonance occurs at $f = 3\,\mathrm{MHz}$ due to an LC resonance or due to an electro-acoustic resonance [26] of the coupling capacitor of the bias-tee.

A correct phase measurement is critical when the capacitance must be derived from an impedance measurement on a non-ideal (dissipating) capacitor.

The practical consequence of the found bias-tee imperfection is illustrated by impedance measurement results of a metal-insulator-metal (MIM) ca-

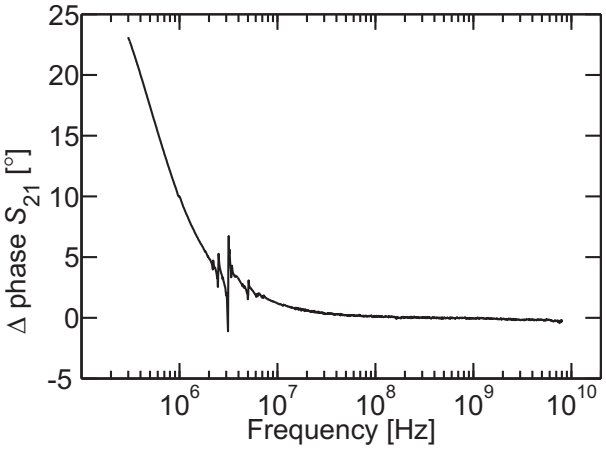


Figure 5.3 – The difference in phase over frequency before and after applying $60V_{\mathrm{dc}}$ voltage stress. The AC power of the VNA was set at $P_{\mathrm{AC}} = 0$ dBm.

pacitor with a 125 nm thick ferroelectric BST layer (see Figure 5.4). A one-port S-parameter measurement was performed on a $30\,\mu$m $\times$ $30\,\mu$m large device electrode from the kHz frequency range up to the low GHz range, using a GSG probe. A SOLT calibration at $V_{\mathrm{dc}} = 0$ V on a Picoprobe CS-5 calibration substrate preceded the actual measurements.

The S-parameters of the 2-port measurement using the VNA were converted to Z-parameters [118] and equation 5.2 was used to extract the series capacitance of the test structure. The measured ferroelectric capacitance shows a typical decrease against increasing frequency at $V_{\mathrm{dc}} = 0$ V (see Figure 5.4). At $V_{\mathrm{dc}} = 5$ V the capacitance reduces below 3 MHz and an unexpected resonance occurs at $f = 3$ MHz.
The measurement results in Figure 5.4 demonstrate that the measurement errors with this particular bias-tee were significant, close to $f = 3$ MHz, due to the *voltage-dependent* resonance of a ferroelectric capacitor in the bias-tee.

At low frequencies a capacitive DUT has a high impedance and hence forms nearly an open-circuit. An open-circuit de-embedding measurement with a DC voltage can drastically reduce the measurement errors. The Y-parameters from the open-circuit measurement at $V_{\mathrm{dc}} = 5$ V were subtracted from the device measurements and the extra error contribution of the voltage-dependency of the bias-tee was successfully removed (see Fig-

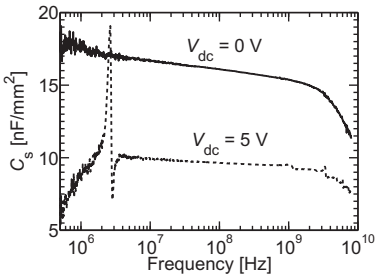


Figure 5.4 – A $30\,\mu\text{m} \times 30\,\mu\text{m}$ BST MIM capacitor with a $h = 125\,\text{nm}$ at $0V_{\text{dc}}$ and at $5V_{\text{dc}}$. A resonance occurs close to $f = 3\,\text{MHz}$ if an electric field is applied.

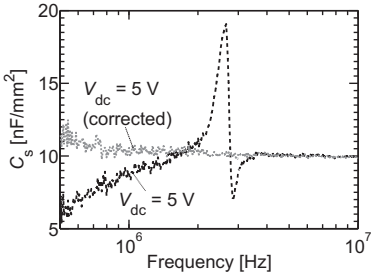


Figure 5.5 – The resonance in Figure 5.4 enlarged. The dotted line shows that the resonance can be removed using an extra open calibration at $V_{\text{dc}} = 5\,\text{V}$.

ure 5.5). A short-circuit and a (precise) $50\,\Omega$ load calibration are not possible due to the excessive DC current that would flow. Voltage-independent capacitors as calibration standards would help, but a voltage-independent bias-tee would be better, since no additional open-calibration is required. This solution is discussed in the following subsection.

5.4.2 A custom made bias-tee

To reduce the measurement errors in the low frequency region, new wide-band high-voltage bias-tees with and without limiters were designed, realized and tested. The new hardware solution uses an NP0-type capacitor. The NP0 classification implies that the capacitor has virtually *no voltage and temperature dependence*. For the development of the new bias-tee a *high voltage* 1206 (large) discrete NP0 capacitor with a custom coplanar waveguide design was used with a simple resistance-capacitance architecture (see Figure 5.6).

The bias-tee schematic with built-in pin diode limiters of Figure 5.6 is shown in Figure 5.7. The limiters were added to protect the VNA from a DC voltage spike, in case the DUT breaks down during measurement. If no high voltages are required during the measurements the diodes can be omitted to improve the transmission path at higher frequencies (this will be exemplified later in Figure 5.11). A Taconix RF TLX laminate substrate was used because of its very low loss ($\tan\delta = 0.0022$ at $f = 10\,\text{GHz}$), low and stable

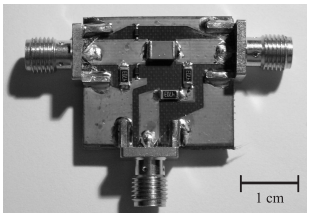


Figure 5.6 – A top view of the newly developed bias-tee.

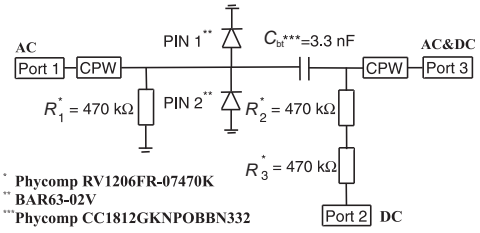


Figure 5.7 – The schematic of the bias-tee with resistors, a large capacitor, PIN diodes and coplanar waveguides (CPW) matched to 50 Ω.

relative dielectric constant $\varepsilon_r = 2.45$, low moisture absorption ($< 0.02\,\%$) and thermal and mechanical stability. A patterned copper layer (35 μm thick) covers the upper side of the laminate; the same copper layer forms a continuous ground plane at the backside.

Three-port measurements were performed to characterize the bias-tees. The results of the new bias-tee with diodes were compared with a commercial wide-band high-voltage Picosecond 5530A-104 bias-tee. The return loss S_{11}, the reverse transmission S_{13}, and the isolation loss S_{12} are shown in Figure 5.8, Figure 5.9, and Figure 5.13, respectively. In Figure 5.11, the magnitude of the transmission S_{13} of the bias-tee with diodes and the one without diodes were compared.

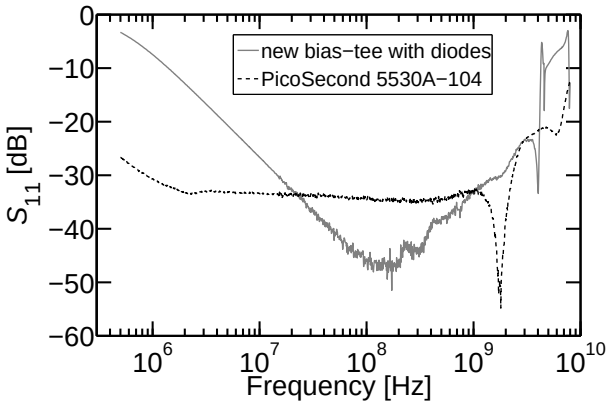


Figure 5.8 – The return loss S_{11} of the new bias-tee with diodes, compared to the commercial bias-tee at $V_{dc} = 0$ V with $P_{AC} = -10$ dBm.

The Picosecond bias-tee has a resistor of $R_{bt} = 1\,\text{k}\Omega$ and a capacitor

of $C_{\mathrm{bt}} = 82\,\mathrm{nF}$, compared to $R_{\mathrm{bt}} = 1$ MΩ of the new bias-tee with a $C_{\mathrm{bt}} = 3.3\,\mathrm{nF}$. The lower capacitance of the new bias-tee is there for two reasons: The amount of stored energy that could damage the equipment at the higher voltage rating of $500\,V_{\mathrm{dc}}$ is lower, and no high-value surface mount ceramic chip capacitors with NP0 characteristic were obtainable for the given physical size.

The new bias-tee has a much higher resistance which results in a lower minimum level of the reflection S_{11} parameter. The capacitance of the new bias-tee, combined with the 50 Ω port resistance explains the high-pass behavior at frequencies below $f = 100\,\mathrm{MHz}$ (see Figures 5.8 and 5.9). At higher frequencies the impedance mismatch and parasitic capacitances of the resistors and limiters increase the return loss S_{11}. The -3dB bandwidth extends from $f = 500\,\mathrm{kHz}$–$3\,\mathrm{GHz}$. Note that the bias-tees without diodes have a wider bandwidth (see Figure 5.11).

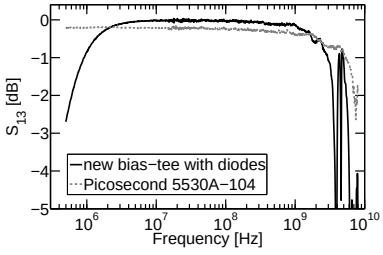


Figure 5.9 – The reverse transmission path S_{13} of the new bias-tees, compared to the commercial bias-tee at $V_{\mathrm{dc}} = 0$ V with $P_{\mathrm{AC}} = $ -10 dBm.

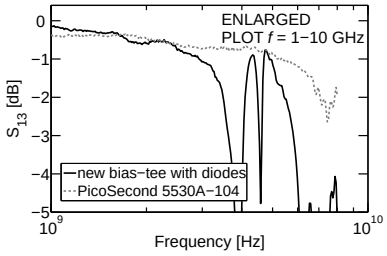


Figure 5.10 – The reverse transmission path S_{13} of the new bias-tees, enlarged in the frequency range of 1–10 GHz.

In Figure 5.13 the DC bias port isolation S_{12} is shown. The insertion loss S_{12} of the Picosecond bias-tee starts constant against the frequency due to its 1 kΩ resistance, then it follows by a low-pass cut-off. The S_{12} of the new bias-tee in Figure 5.13 shows excellent performance up to the resonance around $f = 3\,\mathrm{GHz}$. However, the bias-tee can still be used above the resonance when calibrated, but with reduced accuracy. The increase of the S_{12} at $f = 10\,\mathrm{MHz}$ is due to capacitive coupling to AC ground, probably caused by the resistors and diodes.

A capacitor with an Al_2O_3-based dielectric in a low temperature co-fired ceramic (LTCC) substrate was measured with the new bias-tees at high voltages varying from $V_{\mathrm{dc}} = 0$ to $400\,\mathrm{V}$. The measurement setup is formed

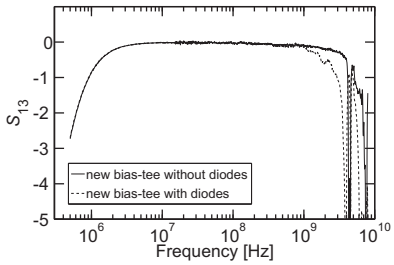


Figure 5.11 – The reverse transmission path S_{13} of the new bias-tees with and without diodes at $V_{dc} = 0$ V with $P_{\mathrm{AC}} =$ -10 dBm.

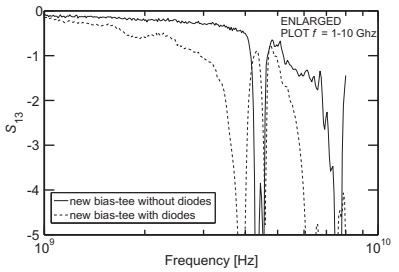


Figure 5.12 – The reverse transmission path S_{13} of the new bias-tees with and without diodes, enlarged in the frequency range of 1–10 GHz.

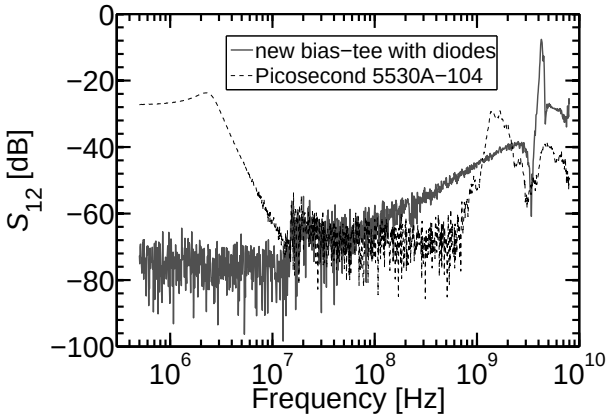


Figure 5.13 – The DC bias port isolation S_{12} of the new bias-tees using a three-port measurement compared to the commercial bias-tee at $V_{\mathrm{dc}} = 0$ V with P_{AC} = -10 dBm at which port 1 = AC signal, port 2 = DC-signal, and port 3 = AC & DC signal.

by a two-port measurement, where one bias-tee on each port, is connected to one probe each. The voltage-independent behavior of the bias-tees, with a capacitor test-structure with a capacitance value of 8.3 pF is shown in Figure 5.14, with respectively $V_{\mathrm{dc}} = 0$ V, 200 V, 400 V, and 0 V once more (i.e. after stress). The shunt capacitor is calculated from a T-equivalent of the Z-parameters of a transmission measurement.

The newly designed bias-tee showed no voltage-dependent behavior up to 400 volt (see Figure 5.14) for the NP0 capacitor embedded in an LTCC substrate. The behavior from $f = 100$ MHz to 8 GHz is affected by the

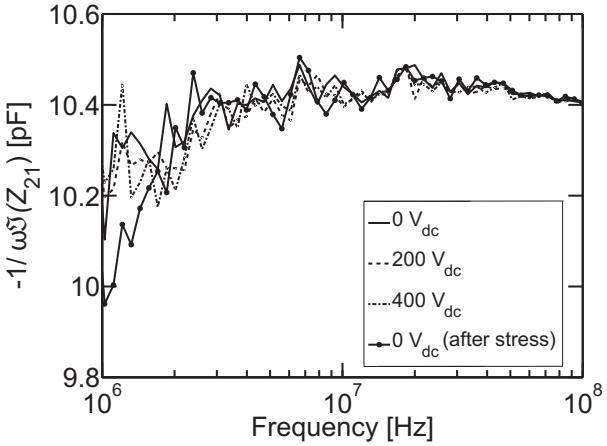


Figure 5.14 – The NP0 capacitance value on an LTCC substrate with an Al_2O_3-based dielectric was determined using impedance parameters, and is measured at room temperature. The plot shows that a change in DC voltage hardly influences the approximated capacitance.

capacitor connections. However, it did not result in resonances nor any bias-dependence (not shown).

5.5 Discussion and conclusions

Determining the relative permittivity and the loss tangent in the kHz-MHz frequency range is crucial for obtaining insight into the quality of the dielectric layers.
During wide-band RF measurements, measurements errors occurred during a voltage-dependent commercial bias-tee. This was circumvented successfully in paragraph 5.4 by:

1) using an additional open calibration to remove the voltage-dependent resonant behavior in the low MHz range caused by the bias-tee, which disturbed the intrinsic response of the DUT, and

2) by designing and developing a voltage-independent bias-tee. The latter hardware solution has much higher resistance values and a much lower coupling capacitance than the commercial bias-tee. Therefore, the S_{11} is high and the S_{31} relatively low at relatively low frequencies. An additional advantage is that the custom bias-tee supports

wide-band high-voltage measurements without an additional open-calibration. Either solution significantly reduces the AC measurement errors in the low Megahertz frequency range.

The content of this chapter has been presented at the IEEE International Conference on Microelectronic Test Structures (ICMTS 2007) [129].

Chapter 6

Ferroelectric capacitor characterization and optimization

6.1 Introduction

In this Chapter, the microstructural and electrical characterization on thin film barium strontium titanate ferroelectric MIM capacitors will be elaborated. Before the start of the research in this work, ferroelectric capacitors already have been optimized for low-frequency applications, using wet-chemical processing of lead zirconate titanate ceramics [101], and are currently being mass-produced, yielding a high throughput, in combination with semiconductor factory-compatible materials.

The research in this work has been performed within a semiconductor company under industrial boundary conditions. With the outlook on a process transfer of barium strontium titanate MIM capacitors, suitable for *radio-frequency* applications, to a semiconductor factory, a process flow using wet-chemical processing was preferred.
The outcome of the material and electrical characterization results on alumina and silicon substrates guided improvements in the process flow. The characterization results mentioned in this dissertation will show the potential of BST (processed with wet-chemical processing) capacitors at RF,

especially in terms of Q and η, and will be useful for RF circuit designers (see Figure 6.19).

This chapter is subdivided in Sections on the sample fabrication, the microstructural characterization, electrical characterization on alumina and silicon substrates, the discussion and is finalized by the conclusions.

6.2 Choice of materials

The MIM capacitor stack is built up by a substrate, metal electrodes and a ferroelectric film. The material choice for each layer will be briefly motivated in the following Subsections.

6.2.1 Substrate

The foundation of the DUT is the substrate. The main requirements for a substrate from a company point of view are: 1) used widely in semiconductor factories (no purchase of new dedicated machines is required) and 2) cost-effective.
In Table 6.1 common substrates in semiconductor production sites with the coefficient of expansion (CTE), the substrate advantages and disadvantages. The CTE of $Ba_{0.7}Sr_{0.3}TiO_3$ (270 nm) film equals $5.2{\cdot}10^{-6}$ [88] and has been determined by a wafer curvature method.

Substrate	**CTE (/ °C)**	**Advantages**	**Disadvantages**
Sapphire	$9.0{\cdot}10^{-6}$ [130]	epitaxial growth of ferroelectrics	expensive (non-common single crystalline material)
Alumina	$5.8{\cdot}10^{-6}$ [88]	good RF isolation, excellent CTE with BST	less common than Si
Single crystalline silicon	$2.7{\cdot}10^{-6}$ [88]	most common semiconductor	CTE mismatch with BST
Glass	$3.2{\cdot}10^{-6}$ [131]	good RF performance	less common than Si

Table 6.1 – The coefficient of thermal expansion (CTE) sapphire, poly-crystalline Al_2O_3 (alumina), single crystalline silicon and glass; and the most important advantages and disadvantages of these substrates.

Barium strontium titanate (BST) has obtained considerable attention by research groups worldwide and can be grown on single crystalline substrates, e.g., Sapphire [102, 103], Magnesium Oxide [132], Lanthanum Aluminate

(LAO) [132], or Strontium Titanate (STO) [133], at high temperatures. However, single crystalline substrates are rather expensive. Cost-effective poly-crystalline substrates are preferred over single crystalline substrates.
BST on ceramic poly-crystalline Al_2O_3 (alumina) substrates was investigated. These substrates are attractive due to the excellent match of the coefficient of thermal expansion (CTE) with BST (see Table 6.1).
A CTE mismatch between the substrate and the film will increase the residual stress caused by thermal strain during heat treatments [83] and can lower the relative permittivity ε_r [88, 89] and tuning ratio η.
Unpolished ceramic substrates are, however, very rough and may result in short circuited capacitors. Therefore, capacitors on top of either polished ceramic substrates or substrates with planarization layers were studied.
BST processed by RF sputtering on top of polished alumina substrates was intensively studied by J. Nath et al. [110] and D. Ghosh et al. [134]. Deposition of BST metal-organic decomposition on alumina substrates with planarization layer is reported by I.P. Koutsaroff et al. [88] for integrated multilayer capacitors.
Furthermore, alumina substrates have a superb isolation, with an electrical resistivity of $>1\,\mathrm{T\Omega{\cdot}cm}$ (even at temperatures as high as 300 °C) [130], resulting in low microwave losses. Clearly, a 'normal' Si substrate has a much lower electrical resistivity ($\lessapprox 1\,\mathrm{k\Omega{\cdot}cm}$) than an alumina substrate ($>1\,\mathrm{T\Omega{\cdot}cm}$ [130]).
Subsequently, capacitors with BST were investigated on silicon (Si) substrates, which are more common substrates to a semiconductor factory. The resistivity can be increased and the electromagnetic field attenuation can be mitigated by using high resistivity Si substrates ($>3\,\mathrm{k\Omega{\cdot}cm}$). Surface passivation can further reduce RF signal losses into the substrate [135, 136].

6.2.2 Metal electrodes

The ferroelectric material is terminated on either side by platinum (Pt). Other metals like Cu, Al, Ag, and Au are less stable to oxidation or have lower melting points and interact faster with the dielectric at high temperatures than Pt [137].
Pt was therefore chosen for the electrode material since it is a noble metal and is known to be resistant to oxidation and corrosion [138]. Pt is known to have a poor adhesion to semiconductor and dielectric substrates [139, 140].

Therefore, glass-planarized alumina and thermally oxidized silicon require an adhesion layer to prevent delamination from the substrate [83]. The most commonly used adhesion layer consists of titanium (Ti) [32, 137, 139, 140].

Investigations on alumina and Si were carried out with Ti/Pt/BST/Pt layers to study the BST properties and growth. It was clear that this stack would not fulfill all application requirements. Low RF losses would require thicker electrodes and low-voltage tuning requires thin dielectric layers. These extra challenges were tackled after the characterization BST was carried out. The Ti adhesion layer was replaced by a TiO_2 layer (see paragraphs 6.4 and 6.5.4) to obtain a good tuning ratio to allow thinner BST layers. Other research groups also opted for a TiO_2/Pt configuration for the bottom metal electrodes [41, 48, 141]. Thicker Pt bottom electrodes were investigated to lower the series resistance and block the Ti diffusion.
Furthermore, the top electrode conductivity was improved by adding a 500 nm thick Au layer on the Pt(100 nm). The Au was added to reduce the sheet resistance and to have a shorter probe landing on the top electrode (faster contact), so that smaller test structures can be measured with improved performance.

6.2.3 Barium strontium titanate

The choice for BST as a ferroelectric material is elaborated in paragraph 3.2. The films, grown under different processing conditions, are investigated by:

a) changing the annealing temperatures to study grain growth and the effect on the ε_r,

b) changing the spinning conditions and to study the effect on the uniformity,

c) changing the dielectric thickness to study influences of dead layers,

d) changing the solid solutions of $SrTiO_3$ to $BaTiO_3$ up to an equal ratio to study the effect on the quality factor Q and the tuning ratio η,

e) adding a small TiO_2 excess to prevent a strong sensitivity to moisture, and

f) adding a cation doping, e.g., Mn^{2+}, Mn^{3+}, Al^{3+}, Fe^{3+}, Cr^{3+}, La^{3+}, etc. [104, 105], to study the affect on Q and η.

In the upcoming sections the processing steps taken will be elaborated further per substrate.

6.3 Sample fabrication

The sample fabrication is outlined for alumina and silicon substrates in the following subsections.

6.3.1 Alumina substrate

The alumina substrate was covered with a 500 nm thick glass-planarization layer. On top of this layer two layers were deposited by sputtering: a thin titanium (Ti) adhesion layer of 10 nm, and a platinum (Pt) layer of 140 nm, which forms a homogeneous bottom electrode.
Successively, $Ba_xSr_{1-x}Ti_{1+y}O_{3+z}$ (BST) films with $x = 0.8$, 0.9 and 1.0 were deposited using wet-chemical processing [142, 143]. Barium titanate solutions were made with $x = 1$, and $y = 0$ and 0.02. Films with 2 at.% Ti excess means that 2 at.% of Ti excess is in the precursor solution, which finally means that the barium strontium titanate films comprise after annealing an excess of 2 at.% TiO_2. We applied solutions with a slight Ti excess to reliably prevent Ba excess in all films, which could result in a strong sensitivity to moisture and thus degrade the performance of the capacitors.
The BST layers were deposited by spin-on technology using wet-chemical processing. The precursors barium and strontium acetates were used for the BST films, and were dissolved in acetic acid. The alkaline earth solution was added to a titanium alkoxide solution, which is formed from titanium iso-propoxide with 1-methoxy-2-propanol as solvent.
Films were spin-coated and the solvent was evaporated on a hot-plate at 150–250 °C for 1–3 minutes. Annealing is carried out at a temperature of 700 °C to crystallize the films during 1–10 minutes. The sputtered 140 nm thick Pt bottom electrode can withstand these high temperatures.
The sputtering of the top electrode takes place at a lower temperature than the annealing temperature. As a top electrode, from the bottom-to-the-top, Pt (100 nm)/Au (500 nm) was applied. Gold (Au) has a higher conductivity and a lower melting point than Pt. Only the top electrode is patterned [114], using dry etching procedures using argon bombardment.

6.3.2 Silicon substrate

The same deposition methods are used as on alumina substrates. However, the layers and layer thicknesses are altered.

The ferroelectric capacitors on top of silicon substrates, were built up as follows. The silicon substrates were thermally oxidized for isolation. Afterwards, the wafers were coated with Ti(20 nm)/Pt(150 nm). The Pt bottom electrode was varied by oxidizing the Ti layer, thickening the Pt layer, or by adding, a Au(500 nm)/Pt(100 nm) layer. The $Ba_xSr_{1-x}Ti_{1.02}O_{3+z}$ was varied from $x = 0.5$ to 0.7, with or without a cation doping. The dielectric layers were between 85 and 280 nm thick and were annealed at temperatures between 680 °C–800 °C during 1–10 minutes. The top electrode consists of a pure Pt(150–200 nm) electrode, or a stacked Pt(100 nm)/Au(500 nm) electrode.

6.4 Microstructural characterization

The growth and properties of thin BST films on glass-planarized alumina, and on silicon substrates were studied. The structural characterization was carried out by Scanning Electron Microscopy (SEM), a Transmission Electron Microscopy (TEM), and by X-ray Diffraction (XRD) analysis. The layer thickness of the thin film BST was typically determined by ellipsometry or by SEM. The results of the microstructural characterization are summarized below.

6.4.1 Alumina substrate

A dielectric thickness of 530 nm ± 12 nm was measured for the reported samples by SEM images obtained from a Philips SEM XL40 FEG.

The thin BST films were grown on top of alumina substrates with a planarization layer, and were extremely fine grained. The grain sizes were in the order of 20–27 nm (see Table 6.2).

Besides an XRD analysis, also a TEM analysis was performed to extract the grain size. A full account of this grain size analysis may be found in [109]. Strong differences in grain size for BST films processed at the

BST composition	**Scherrer {110}**
$BaTiO_{3+z}$	25.6 ± 0.7 nm
$BaTi_{1.02}O_{3+z}$	22.4 ± 0.6 nm
$Ba_{0.9}Sr_{0.1}Ti_{1.02}O_{3+z}$	20.4 ± 0.5 nm
$Ba_{0.8}Sr_{0.2}Ti_{1.02}O_{3+z}$	19.7 ± 0.6 nm

Table 6.2 – The grain size with XRD is determined using Scherrer's formula [144]. The deviations (±) for XRD indicate the statistical accuracy of the mean value, not the width of the crystallite size distribution.

same processing temperature were not observed (see Table 6.2). The grain size analysis indicates, that with decreasing barium content in the BST films with 2 at.% excess titanium oxide, there is a slight decrease of the grain size by 10 %.

A slightly larger grain size of 49 nm was reported for BST films reported by I.P. Koutsaroff et al. [145]. The latter consisted of a BST film with 70 at.% barium grown on alumina with a planarization layer, processed by metalorganic deposition at temperatures of 685 °C. A. Ioachim et al. [102] processed BST with 50 at.% Ba by pulsed laser deposition, on sapphire and alumina substrates. To improve granular growth, doping with MgO and MnO_2 was applied [146]. These BST films were also annealed at high temperatures of 800 °C, and the XRD analysis shows grain sizes of 50–60 nm.
Experimental results of thin BST films have shown that a lower grain size distribution results in a lower temperature sensitivity of the ε_r [82–84].

6.4.2 Silicon substrate

The layer stack on silicon substrates was almost identical to the one on alumina, except for a small thickness increase of the Ti adhesion layer (20 nm instead of 10 nm). The X-ray analysis indicates a small grain size of ca. 20 nm in the BST on silicon, comparable to the grain size of the BST on alumina substrates (see Table 6.2). Through electrical characterization, it was discovered that the Ti/Pt bottom electrode affects the electrical performance. An Energy Dispersive X-ray (EDX) line profile analysis, throughout the complete layer stack, showed that a 130 nm BST film grown on a Ti/Pt bottom electrode contains a thin TiO_2 dead interface layer *above* the Pt bottom electrode (see Figure 6.1).

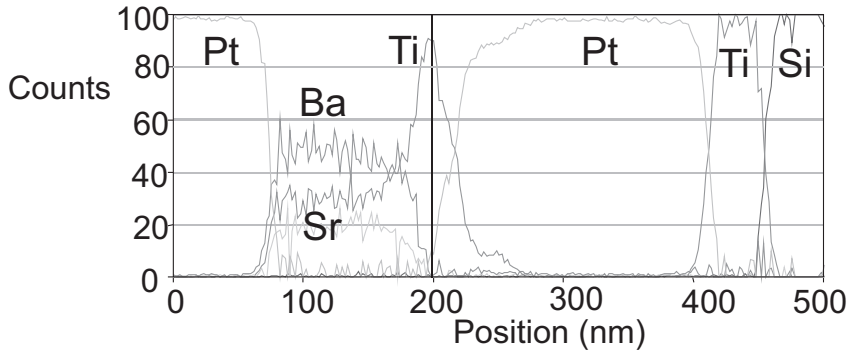


Figure 6.1 – EDX analysis performed across the complete stack indicating that a TiO_2 layer exists above the Ti/Pt bottom electrode.

Titanium diffuses through the Pt, which is consistent with electrode material studies by J.O. Olowolafe et al. [139] and by A. Erlich et al. [140]. Titanium diffused through the Pt and formed a TiO_2 dead layer with a lower dielectric constant than BST. Consequently, the relative permittivity decreases with this thin incorporated interfacial layer with a low relative permittivity between 70–80 (see [147, 148]).

To minimize the dead layer, BST was processed with a TiO_2 layer, instead of a Ti layer below the bottom electrode. Homogeneous dense films with a sharp Pt-BST interface were confirmed by an EDX analysis. No Ti enriched layer could be detected by TEM between the bottom Pt layer and the BST layer (see Figure 6.2).

Electrical characterization of ferroelectric capacitors in the next section will show that the measured ε_r of a MIM capacitor with a the TiO_2/Pt bottom electrode increases notably compared to a capacitor with Ti/Pt processed under identical conditions.

6.5 Electrical characterization

Thin film MIM ferroelectric capacitors were investigated as a function of temperature, frequency and electric field. Typically square shaped test structures are used for the low frequency measurements and circular shaped test structures (as shown in Figure 4.1) for the RF measurements.

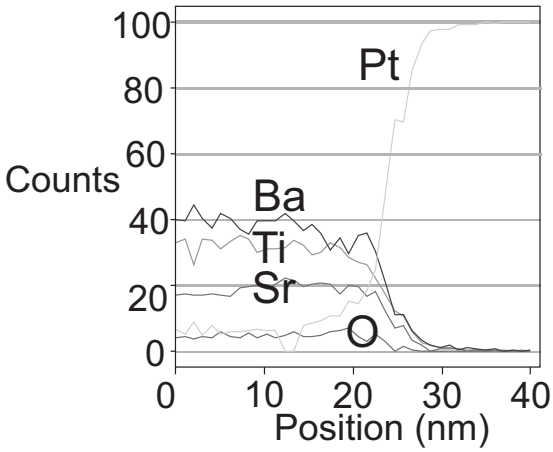


Figure 6.2 – EDX analysis performed through a BST sample processed with a TiO_2/Pt bottom electrode. In this example the EDX scanned from the bottom section of the BST to the underlying bottom electrode.

In this Section the dependency of the ε_r and the $\tan\delta$ on processing conditions and the dielectric response to temperature, frequency and voltage sweeps are presented and discussed.

6.5.1 Dependence of the relative permittivity on processing conditions

The uniformity of the dielectric layers of the measured MIM capacitors and the annealing temperature of the BST will be discussed.

Uniformity

The homogeneity of the thin solid films was measured across the wafer with an impedance analyzer (see Section 4.3.1). The total signal electrode area of the capacitors was approximately $10.000\,\mu m^2$. Electrical characterization of the capacitance values shows that the dielectric layer uniformity was improved from $\pm 10.5\,\%$ to $\pm 2\,$at.% capacitance deviation, in a research environment, by changing the deposition conditions.

Dielectric annealing temperature

To study how much influence the annealing temperature and the thickness of the film have on the ε_r and $\tan\delta$ several experiments were performed at 680, 740 and 800 °C at different dielectric thicknesses (see Figure 6.3).

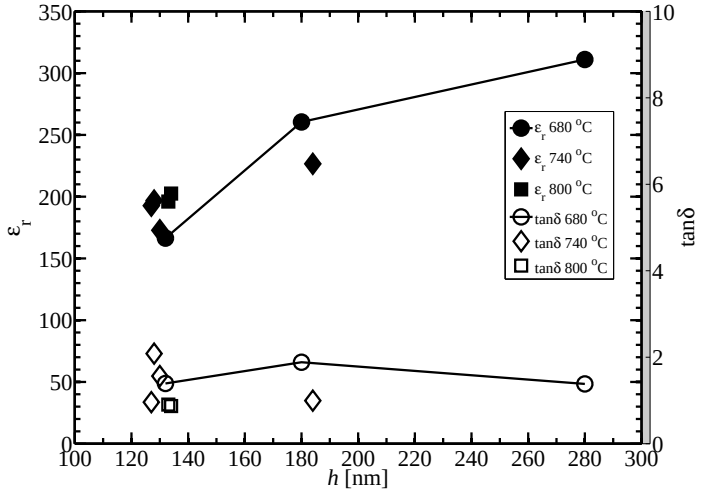


Figure 6.3 – The ε_r and $\tan\delta$ for 3 dielectric annealing temperatures versus dielectric thickness h. The $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ capacitors were realized on Si, and measured on a physical area of $100\,\mu m \times 100\,\mu m$ at 1 MHz, 50 mV_{ac}, zero DC bias and at ambient temperature. The BST has Pt top and Ti/Pt bottom electrodes.

The ε_r increases with dielectric thickness. In a Ti/Pt/BST/Pt stack an interface layer is present above the Ti/Pt bottom electrode (see Figure 6.1). As a result, the ε_r increases with increasing annealing temperature of the BST. The loss tangent was almost unaffected by the dielectric layer thickness.

6.5.2 Electrical properties versus ambient temperature

Capacitors integrated in mobile phones are exposed to different environment temperatures. Therefore, it is important to investigate the response of the capacitors to the temperature.

To measure the sensitivity of the ε_r and $\tan\delta$ of the processed fine-grained BST thin films the operation temperature is varied from -160 to at least a 180 °C. Preferably, the ε_r variation with temperature is low and the loss tangent should be as low as possible in RF applications.

6.5.2.1 Alumina substrate

The relative permittivity ε_r of all BST compositions on alumina in response to the temperature sweep is shown in Figure 6.4.

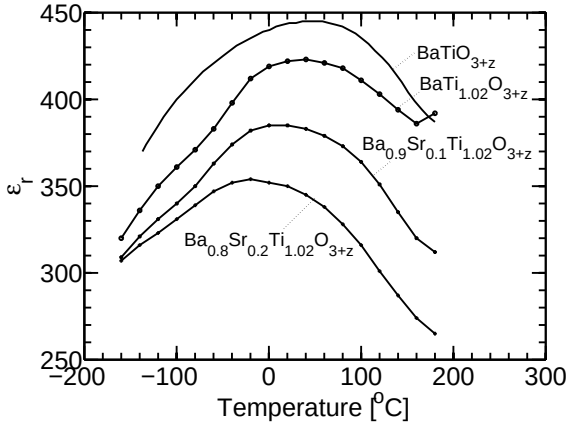


Figure 6.4 – The relative permittivity plotted against the temperature for BST samples on alumina measured on an area $A = 275.000\ \mu m^2$ at 100 kHz, zero DC bias, and $0.1\,V_{ac}$. A decrease in barium content in BST shifts and reduces the peak of the relative permittivity.

The temperature response curve is typical for ferroelectric thin films (see Chapter 3).

Measurement data of the samples on alumina show that the 530 nm thin BST films resulted in a broad relative permittivity plateau $T_{\varepsilon_{r,max}}$ at the Curie temperature (see Figure 6.4). The measured data in Figure 6.4 shows the shift of the Curie temperature with decreasing Ba content and is consistent with the work of others [84, 86, 149]. The lower ε_r compared with bulk ceramics and the broad Curie maximum is attributed to the grain sizes and interfacial layers for thin film capacitors, which are for all compositions in the order of 20–30 nm, e.g., compared to the much larger grain size differences in [149] of 1 μm, 1.5 μm and 10 μm for sintered (at much higher

temperatures) $BaTiO_3$ hot-pressed ceramics.

The temperature at the maximum relative permittivity for the barium titanate films without strontium content has been determined to be 45–50 °C (see Figure 6.4). The relative permittivity is the highest for the barium titanate layer without titanium oxide excess and achieved a value of 460 at 21 °C at a 100 kHz and 50 mV_{ac}. A slight titanium oxide excess of only 2% in the barium titanate film results in approximately 10 % lower measured relative permittivity of 420 at 21 °C, and 100 kHz.
S.K. Streiffer et al. [106] and S. Stemmer et al. [150] investigated respectively 30 nm thick and 20–160 nm thick $Ba_{0.7}Sr_{0.3}Ti_{1+y}O_{3+z}$ films grown by chemical vapour deposition, applying a Ti excess of y = 0.04–0.15. This is a much higher Ti excess compared to our films. A reduction of the relative permittivity for 150 nm thick films of more than 25 % is measured, if a Ti excess of 10 at.% is applied. STEM studies in [150] revealed that a low Ti excess of only 4 at.% is accommodated in the grain interiors, whereas higher Ti excess in the films results in partial accommodation in the grain interiors and partially at the grain boundaries.

In this work, the measured BST films with 80 and 90 at.% barium, processed with 2 at.% Ti excess shifted the maximum relative permittivity from 45 °C for the pure barium titanate film to 20 °C for $Ba_{0.9}Sr_{0.1}Ti_{1.02}O_{3+z}$ and -20 °C for $Ba_{0.8}Sr_{0.2}Ti_{1.02}O_{3+z}$, which corresponds to a shift of the broad Curie temperature of 3.6 degree per at.% strontium [8].

The micro-structure of the ceramic is affecting the temperature dependency of the relative permittivity. Thin fine-grained films have a broad maximum around T_c (see Figure 6.4). In contrast, a larger average grain size, e.g., in the case for single crystalline $SrTiO_3$ [80], results in an $\varepsilon_r(T)$ curve with a higher, steeper peak, i.e., a much stronger temperature dependence of the relative permittivity.
In Figure 6.4 the maximum relative permittivity is shifted with Ba content, as known from single crystalline data and bulk ceramics (see Figure 30 in [81] and [23]). Furthermore, the Curie maximum plateau is broad for all thin films and the maximum value is lower compared to the value of the related bulk ceramics. This is also reported by other groups [86] and explained by interface layers with reduced permittivity and Curie temperature.

The loss tangent against the temperature is depicted in Figure 6.5.

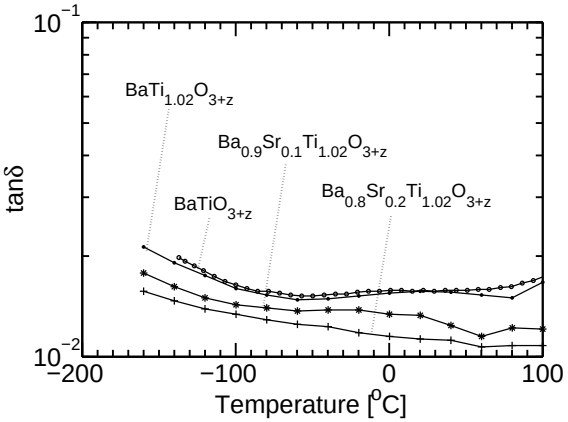


Figure 6.5 – The loss tangent $\tan\delta$ plotted against temperature for the BST samples on alumina, measured on an area $A = 275.000\,\mu\text{m}^2$ at 100 kHz, zero DC bias, and 0.1 V_{ac}.

All BST thin films with barium content of 80–100 at.%, with as well as without titanium excess, result in a loss tangent of 1.1–2.1 % up to a 100 °C. The lowest $\tan\delta$ is obtained for the BST film with the lowest Ba content. The loss tangent is essentially constant across the full temperature range and especially in the application range from -50 °C to 100 °C. No peak as with bulk ceramics is obtained due to the very fine-grained (20–26 nm) polycrystalline BST thin films.

6.5.2.2 Silicon substrate

The material studies were furthermore carried out on silicon substrates to improve the $Q(\eta)$ at RF (see Section 6.3.2).

The measured circular large test structures consist of an area of about $2.75\times10^{-7}\text{m}^2$ and are measured at 100 kHz, 0.1 V_{ac} and 0 V_{dc}. The measured temperature response of 110 nm thick $Ba_{0.5}Sr_{0.5}Ti_{1.02}O_{3+z}$ and 115 nm thick $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ samples, with and without cation doping[1], including a thicker 200 nm Pt bottom electrode, are visualized in Figure 6.6.

The temperature at the maximum relative permittivity decreases with less barium in the BST.

[1] Company Confidential.

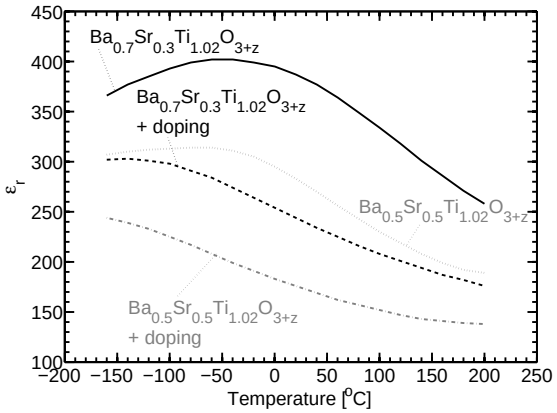


Figure 6.6 – The measured ε_r(T) for the 110 nm thick $Ba_{0.5}Sr_{0.5}Ti_{1.02}O_{3+z}$ and $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ layers with and without doping.

Figure 6.6 shows that cation doping in BST decreases the Curie temperature even further, making the material more paraelectric (see Section 3.1).

6.5.3 Small-signal properties versus frequency

To study the frequency response of the relative permittivity, the total loss tangent and the dielectric loss of our thin film BST MIM capacitors for RF applications, measurements were performed from 100 kHz up to 8 GHz.

The performance of the ε_r, $\tan\delta$, Q, and Q_{intr} are of interest to, e.g., RF circuit designers.

6.5.3.1 Alumina substrate

At low frequencies an impedance analyzer was used (see Section 4.3) to measure the ε_r and $\tan\delta$. Each parameter was measured on a 250 μm × 250 μm capacitors at zero DC bias, ambient temperature and 50 mV_{ac} (see Figure 6.7).

Figure 6.7 (on the left) shows the decreases of the ε_r with frequency. The $BaTiO_{3+z}$ sample with the strongest ferroelectricity at ambient temperature shows a faster decrease of the ε_r with frequency, compared to the other samples.

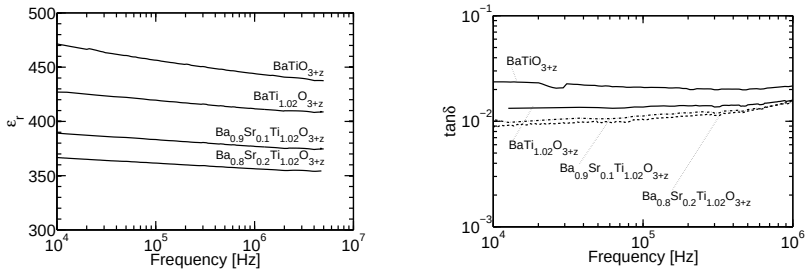


Figure 6.7 – The ε_r and $\tan\delta$ of BST compositions on alumina measured on $250\,\mu m \times 250\,\mu m$ capacitors at zero DC bias, ambient temperature and $50\,mV_{ac}$. Above 1 MHz the $\tan\delta$ increases due to resistive electrode losses (not shown).

Figure 6.7 (on the right) indicates that the pure $BaTiO_3$ film has losses of 2 at.% at 100 kHz (and at ambient temperature). The $BaTiO_3$ film with Ti excess shows a slightly lower loss of 1.5 %. The BST films with barium content of $x = 0.8$–0.9 % show lower Curie temperatures, than the pure $BaTi_{1+y}O_3$ with $y = 0$ or 0.02 and lower losses of 1.0 %.

To verify if the low and high frequency measurements are comparable, since the measured frequency band overlaps, a wide-band frequency analysis is performed for the ε_r and $\tan\delta$. A wide-band frequency analysis of the relative permittivity across 8 orders of magnitude is depicted in Figure 6.8. Relatively large capacitors with areas of $250\,\mu m \times 250\,\mu m$ and a signal pad diameter of $88\,\mu m$ were tested, with respectively an impedance analyzer and a VNA, to minimize noise. Small capacitors at RF with a signal pad diameter of $8\,\mu m$ were measured with a VNA, to reduce the resistive electrode losses.

In Figure 6.9 the loss tangent is given for a $250\,\mu m \times 250\,\mu m$ $BaTi_{1.02}O_3$ MIM capacitor measured by the impedance analyzer, and additionally circular RF test structures with a signal pad diameter $d = 88$, 24, and $8\,\mu m$ were measured using a VNA.

The data of the impedance analyzer and VNA were combined to show the typical broadband $\tan\delta$ response with frequency. The $\tan\delta$ was relatively flat around 1.4 % up to almost 100 MHz, and below 5 % up to 1 GHz. In or close to the GHz frequency range the losses increase due to the electrodes. The low frequency and high frequency (VNA) measurements of the ε_r and $\tan\delta$ overlap, which gains confidence in the RF measurement results.

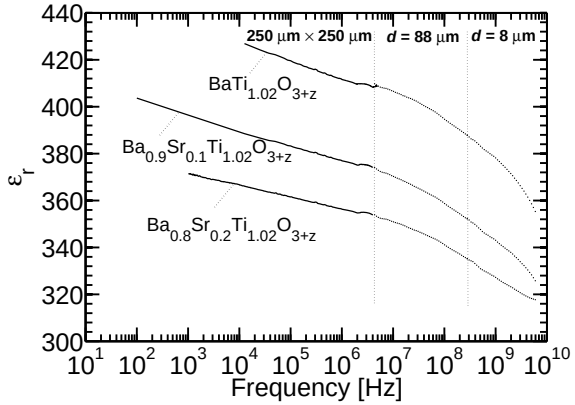


Figure 6.8 – The relative permittivity of capacitors of the $Ba_{0.8}Sr_{0.2}Ti_{1.02}O_{3+z}$, $Ba_{0.9}Sr_{0.1}Ti_{1.02}O_{3+z}$ and $BaTi_{1.02}O_{3+z}$ samples on alumina against frequency across 8 orders of magnitude. The data has been obtained from the impedance analyzer ($250\,\mu m \times 250\,\mu m$ capacitors measured at 50 mV_{ac}) and from the VNA (circular capacitors with a signal pad diameter of $d = 88\ \mu$m and $d = 8\ \mu$m were measured at -10 dBm RF power, zero DC bias and at ambient temperature).

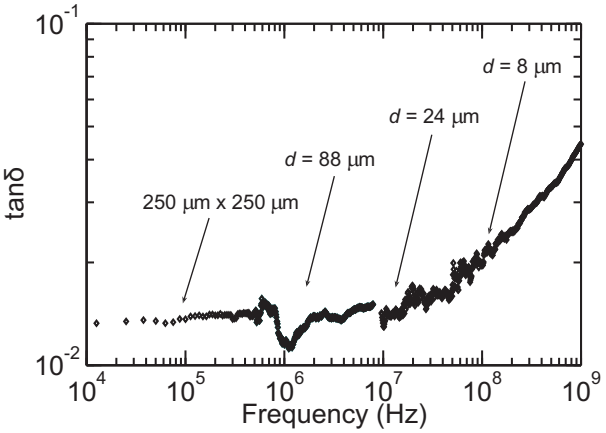


Figure 6.9 – The broadband frequency response of $\tan\delta$ of a relatively large $250\,\mu m \times 250\,\mu m$ $BaTi_{1.02}O_{3+z}$ MIM capacitor, measured on an impedance analyzer at 50 mV_{ac}, and circular RF circular DUTs with a signal pad diameter $d = 88$, 24 and 8 μm were measured on a VNA at -10 dBm RF power, zero DC bias and at ambient temperature.

The measured Q at 1 GHz, as a function of barium content in the BST thin films, is depicted in Figure 6.10 for the samples with Ti excess.

At 1 GHz the BST films with Ti excess, grown on planarized alumina

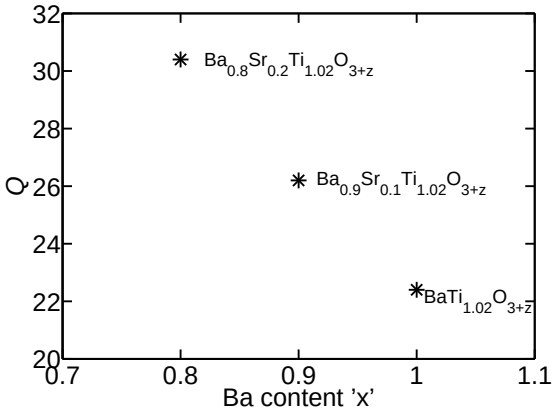


Figure 6.10 – The total quality factor at 1 GHz performed on circular GSG RF structures with a signal pad diameter of 8 μm for BST compositions on alumina at -10 dBm, zero DC bias and at ambient temperature.

substrates and processed under same processing conditions, show quality factors of 22 for $BaTi_{1.02}O_{3+z}$, 26 for $Ba_{0.9}Sr_{0.1}Ti_{1.02}O_{3+z}$, and 30 for $Ba_{0.8}Sr_{0.2}Ti_{1.02}O_{3+z}$. The measured data is comparable to data reported in literature for sputtered and chemical solution deposition (CSD) deposited BST MIM capacitors with 70 at. % Ba, processed on alumina substrates with a SiO_2 layer. I.P. Koutsaroff et al. [40] report quality factors of 20–30 at 1 GHz.

The frequency response measurements on alumina point out that our cost-effective process flow has lead to ferroelectric capacitors with state-of-the-art quality factors at 1 GHz.

6.5.3.2 Silicon substrate

Along the route of optimization, the bottom electrode was improved by a TiO_2 adhesion layer below the bottom electrode, as discussed in paragraph 6.4. The TiO_2/Pt bottom electrode influences the permittivity. The wafers contain a Ti/Pt bottom electrode with a 130 nm thick $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ film on top had an $\varepsilon_r = 173$ at 1 MHz and the wafer with the TiO_2/Pt sample contained a $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ film of 115 nm had an $\varepsilon_r = 405$ at 1 MHz. The permittivity increased more than a factor of 2 using a TiO_2 layer below the Pt bottom electrode on silicon.

The response of the Q $(=1/\tan\delta)$ decreases with frequency as was shown in Figures 4.9 and 6.9. The Q and the Q_{intr} at 1 GHz of the $Ba_{0.5}Sr_{0.5}Ti_{1.02}O_{3+z}$ and $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ samples, with and without cation doping, are depicted in Figure 6.11.

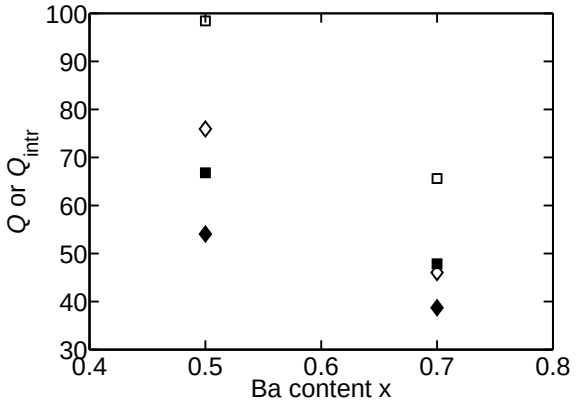


Figure 6.11 – The Q and Q_{intr} at $f=1$ GHz for $d=8\,\mu$m signal pad GSG MIM capacitors for $Ba_{0.5}Sr_{0.5}Ti_{1.02}O_{3+z}$ and $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ samples with and without cation doping on Si. The open markers indicate the intrinsic quality factor (Q_{intr}), the closed markers indicate the total quality factor Q, the diamond markers indicate the $Ba_xSr_{1-x}Ti_{1.02}O_{3+z}$ without cation doping, and the squared indicates the $Ba_xSr_{1-x}Ti_{1.02}O_{3+z}$ with cation doping.

Total quality factors Q between 39–76 were achieved at 1 GHz for the BST samples on Si with a TiO_2/Pt bottom electrode and Pt(100 nm)/Au(500 nm) top electrodes. The intrinsic quality factor Q_{intr}, that exclude electrode losses (see paragraph 4.2.5), varied from 48–98 at 1 GHz.

6.5.4 Q and η versus electric field

Besides the quality factor Q, the tuning ratio η is also a key property of ferroelectric capacitors. In the following paragraphs, these measured performance parameters are presented for alumina and silicon substrates.

6.5.4.1 Alumina substrate

$100\,\mu\mathrm{m}\times 100\,\mu$m and $250\,\mu\mathrm{m}\times 250\,\mu$m test structures were measured during an upwards DC voltage sweep at 1 MHz and 50 mV_{ac}. A positive DC voltage

is applied on the bottom electrode with the top electrode at $0\,V_{\mathrm{dc}}$.

The tuning of the relative permittivity with electric field is depicted in Figure 6.12 and is limited by the measurement equipment to $|E| = 0.4$ MV/cm.

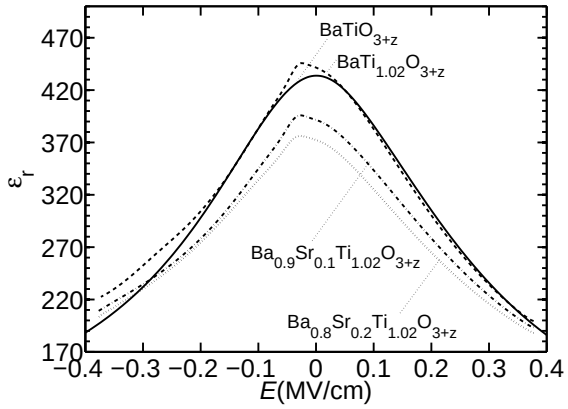


Figure 6.12 – The relative permittivity with electric field of the Ti/Pt/BST/Pt/Au samples on alumina during an upwards DC voltage sweep. The $100\,\mu\mathrm{m} \times 100\,\mu\mathrm{m}$ test structures were measured at 1 MHz, $50\,\mathrm{mV_{ac}}$ and at ambient temperature. The relative permittivity decreases with a lower amount of barium and with increasing absolute electric field.

The closer the operating temperature is to T_{c}, the larger the relative permittivity will be (see Figures 6.4 and 6.12).

The relationship between the tuning ratio and the barium content in $\mathrm{Ba_xSr_{1-x}Ti_{1+y}O_{3+z}}$ at 0.4 MV/cm (20 $\mathrm{V_{dc}}$) is shown in Figure 6.13 for all compositions on alumina.

The tuning ratio η ($E = 0.4$ MV/cm) was between 1.8 (low barium content in BST)–2.2 (high barium content in BST).

The loss tangent with electric field is determined and depicted in Figure 6.14.

The $\mathrm{BaTiO_3}$ sample, which is in the ferroelectric phase (ambient temperature $< T_{\mathrm{c}}$) shows a hysteresis, by means of a bump close to zero electric field, resulting in an additional increase in loss tangent, and an increase in zero DC bias relative permittivity due to switching of the spontaneous polarization. All other samples were mainly in the paraelectric phase (ambient temperature $> T_{\mathrm{c}}$), and have reduced hysteresis effects, a lower relative permittivity and loss tangent.

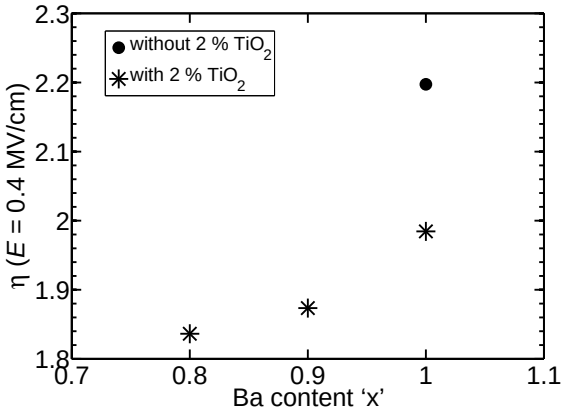


Figure 6.13 – The tuning ratio at an electric field of at $E = 0.4\,\mathrm{MV/cm}$ in relation to the amount of Ba in $Ba_xSr_{1-x}Ti_{1.02}O_{3+z}$ at 1 MHz, at ambient temperature, and an AC voltage of $50\,\mathrm{m}V_{ac}$.

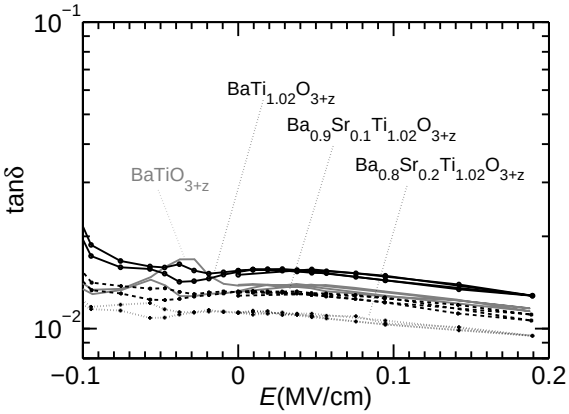


Figure 6.14 – The loss tangent with electric field of BST on alumina samples measured at 100 kHz at ambient temperature in the cryostat.

6.5.4.2 Silicon substrate

The BST layers on Si were typically more than half as thin as the 530 nm thick samples on alumina. The dielectric composition, dielectric thickness, and electrodes were adapted with the aim to improve performance on Si. Albeit, the C_s, Q, Q_{intr}, η and R_s changed accordingly. The resistivity of 'normal' Si substrate will also add to the losses. The consequences for the Q and η with electrical field strength E were studied.

The quality factor is dependent on the capacitance. An increase in E reduces the capacitance and increases the Q at higher frequencies (see equation 4.9). A typical example is given for a $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ composition on Si in Figure 6.15.

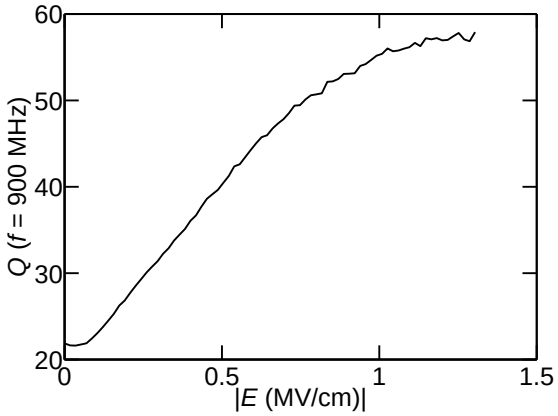


Figure 6.15 – The total quality factor including resistive loss versus electric field at $f = 900\,\mathrm{MHz}$.

The worst-case Q of a ferroelectric capacitor in an application is typically obtained at zero DC bias. Therefore, we specify the Q of a device at zero DC bias. With an increasing absolute E the Q improves at high frequencies.

Besides the total Q, the electrodes can influence the tuning ratio, as addressed in Section 6.4.

The electrical characterization results of the measured capacitance density against electric field adds strength to the EDX results in Figures 6.1 and 6.2, which showed that a TiO_2 interface layer does not co-exist in the BST in the case of a TiO_2/Pt bottom electrode, since the measured $\varepsilon_r(0\,V_{dc})$ increases more than a factor of 2 for the sample with a TiO_2/Pt bottom electrode, as depicted in Figure 6.16. The thickness of the interface layer was estimated by taking the difference of the capacitance density and using an $\varepsilon_r = 80$ [148]. Respectively, the interfacial TiO_2 layer thickness is estimated at 45 nm, which is supported by the EDX analysis results in Figures 6.1 (constant counts) and 6.2.
At CMOS compatible operating voltages of $3\,V_{dc}$ these high quality thin films on Si show already tuning ratios of 1.7 for the TiO_2/Pt sample (see Figure 6.16). Note that $3\,V_{dc}$ is much lower than the maximum electrical

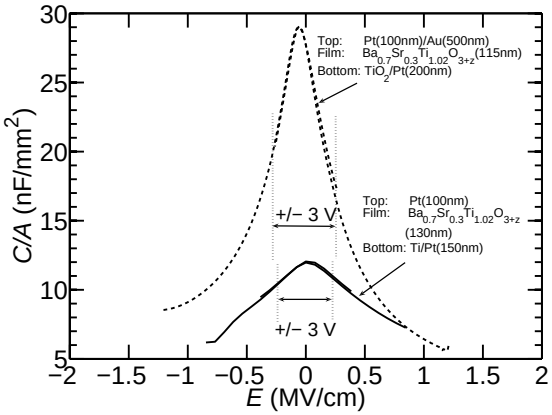


Figure 6.16 – The tuning ratio decreases due to a TiO_2 interface layer in the case of a Ti/Pt bottom electrode, indicated by measurements on two different samples annealed at 740 °C. The up/down sweep was scaled to $\varepsilon_r(0\,V_{dc})$.

field strength.

The work on the improved performance of the TiO_2/Pt bottom electrode in relation to the tuning ratio at low operating voltages has been published in the IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control journal [101].

After the bottom electrode was improved, optimization of the Q was continued. Firstly, the dielectric solution was fine-tuned by lowering the barium content further to $Ba_{0.5}Sr_{0.5}Ti_{1.02}O_{3+z}$. Secondly, a cation cation doping was added to the BST having the same electrodes as the former. The tuning ratio is demonstrated by plotting $\varepsilon_r(E)$ in Figure 6.17.

Less barium yields a reduced T_c (see Figure 6.6), making the dielectric more paraelectric at room temperature, and hence, decreasing the ε_r and η (see Section 3.3).

The intrinsic Q_{intr}, i.e., the reciprocal of the dielectric loss $\tan\delta_\varepsilon$ (see equation 4.9), is depicted in Figure 6.18 at $0\,V_{dc}$ (worst case Q; see also equation 4.9), with and without cation doping with the $\eta(5\,V_{dc})$ for $Ba_{0.5}Sr_{0.5}Ti_{1.02}O_{3+z}$ and $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$.

Changing from a $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ film to a $Ba_{0.5}Sr_{0.5}Ti_{1.02}O_{3+z}$ film increases Q_{intr} respectively from 48 to 67 at 1 GHz. An additional cation doping boosts the Q_{intr} respectively from 66 up to 98. An additional cation

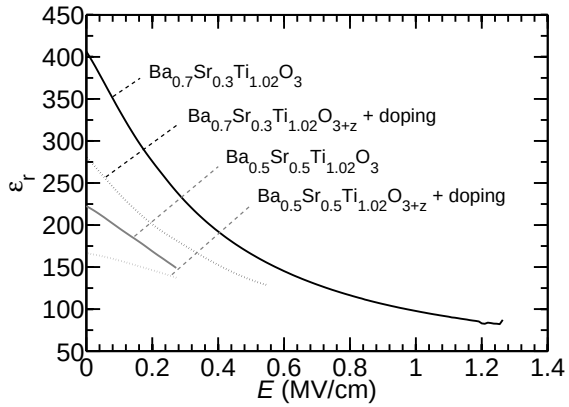


Figure 6.17 – The $\varepsilon_r(E)$ response curves of 100 μm × 100 μm capacitors measured at 1 MHz and 50 mV_{ac} show the influence of 110 nm thick $Ba_{0.5}Sr_{0.5}Ti_{1.02}O_{3+z}$ and $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ films with and without cation doping.

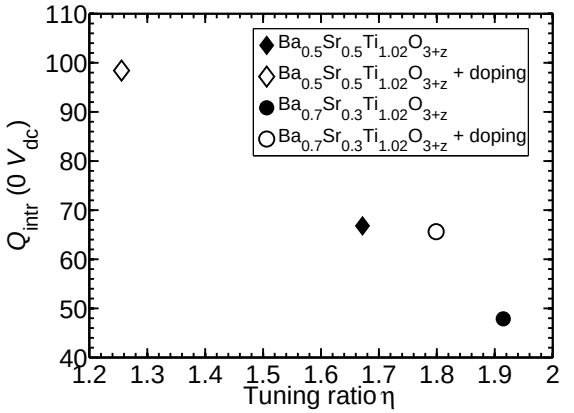


Figure 6.18 – The intrinsic Q at 0 V_{dc} of the $Ba_{0.5}Sr_{0.5}Ti_{1.02}O_{3+z}$ and $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ samples on Si, with and without cation doping, at 1 GHz and -10 dBm RF power. The η is measured at 5 V_{dc} ($E = 0.45$ MV/cm) on 100 μm × 100 μm capacitors at 50 mV_{ac}.

doping has the same impact as reducing the Ba content in BST. Both approaches prove to be effective in raising Q_{intr}, but lower the tuning ratio η.

Figure 6.18 clearly shows the interplay between Q_{intr} and η. By depositing a different BST composition a tunable capacitor can be realized, which has a high Q or a high η for an application.

The aforementioned electrical measurements are essential to show the potential of ferroelectric capacitors.

6.6 Discussion

The Q and η at a specified operating (radio) frequency should be as high as possible. As discussed in Chapter 2 and paragraph 6.5.4 a $Q(\eta)$ trade-off exists.

$Q(\eta)$ measurement data on BST MIM capacitors on alumina and silicon substrates from this work and from other research groups are summarized in Figure 6.19 and discussed. Details of the MIM capacitors are summarized in Table 6.3. The maximum reported tuning ratio η was used in Figure 6.19. All measured data points from this work are determined at the maximum operating voltage of the measurement equipment (relatively thick samples on alumina) or of the device.

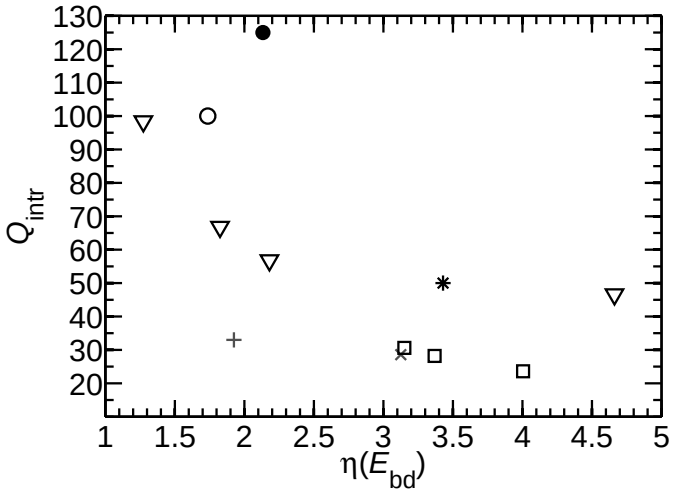


Figure 6.19 – The $Q_{\mathrm{intr}}(\eta)$ datapoints on silicon and alumina substrates of ferroelectric capacitors. The experimental data has been obtained from literature and from this work. The markers are indicated in the last column of Table 6.3. The Q_{intr} together with its $\eta(E_{\mathrm{bd}})$ could not be retrieved from [40, 151], therefore the (total) Q is given with respectively the gray symbols 'X' and '+'. The squared and triangular markers show measurements, respectively on alumina and silicon substrates, from this work.

Substrate and bottom electrode	**Composition, dielectric thickness and deposition technique**	Top electrode	Q_{intr}**(0** V_{dc}**) measured at**	$\eta=\frac{\varepsilon_r(0\,V_{\mathrm{dc}})}{\varepsilon_r(E_{\mathrm{bd}})}$	**Source, symbol**
$Al_2O_3/SiO_2/TiO_x/Pt$	$Ba_{0.7}Sr_{0.3}TiO_3$ (140 nm, CSD)	Pt(200 nm)	$Q=29$ (1 GHz)	3.1	[40], x
Al_2O_3/glass/Ti/Pt	$Ba_{0.8}Sr_{0.2}Ti_{1.02}O_{3+z}$ (530 nm, wet-chemical processing)	Pt(100 nm)/Au(500 nm)	31 (1 GHz)	3.2	this work, □
Al_2O_3/glass/Ti/Pt	$Ba_{0.9}Sr_{0.1}Ti_{1.02}O_{3+z}$ (530 nm, wet-chemical processing)	Pt(100 nm)/Au(500 nm)	28 (1 GHz)	3.4	this work, □
Al_2O_3/glass/Ti/Pt	$BaTi_{1.02}O_{3+z}$ (530 nm, wet-chemical processing)	Pt(100 nm)/Au(500 nm)	24 (1 GHz)	4.0	this work, □
high-res $Si/SiO_2/TiO_2/Pt/Au/Pt$	$Ba_{0.25}Sr_{0.75}TiO_3$ (300 nm, PLD)	Pt(50 nm)/Au(500 nm)	100 (10 GHz)	1.7	[41], o
$Si/SiO_2/IrO_2/Pt$	$Ba_{0.7}Sr_{0.3}TiO_3$ (300 nm, MOCVD)	Pt(300 nm)	125 (0.045–0.5 GHz)	2.1	[111], *
$Si/SiO_2/TaSiN/TaSiN_xO_y/Pt$	$Ba_xSr_{1-x}Ti_{1+y}O_{3+z}$ (30 nm, MOCVD)	Pt(50 nm)	$Q=33$ (1 GHz)	1.9	[151], +
$Si/SiO_2/TiO_2/Pt$	$Ba_{0.6}Sr_{0.4}TiO_3$ (300 nm, RF magn.sputt.)	Pt(400 nm)	50 (0.001 GHz)	3.4	[48], •
$Si/SiO_2/TiO_2/Pt$	$Ba_{0.5}Sr_{0.5}Ti_{1.02}O_{3+z}$ (110 nm, wet-chemical processing)	Pt(50 nm)/Au(500 nm)	67 (1 GHz)	1.8	this work, ∇
$Si/SiO_2/TiO_2/Pt$	$Ba_{0.5}Sr_{0.5}Ti_{1.02}O_{3+z}$ + doping(110 nm, wet-chemical processing)	Pt(50 nm)/Au(500 nm)	98 (1 GHz)	1.3	this work, ∇
$Si/SiO_2/TiO_2/Pt$	$Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ (115 nm, wet-chemical processing)	Pt(50 nm)/Au(500 nm)	47 (1 GHz)	4.7	this work, ∇
$Si/SiO_2/TiO_2/Pt$	$Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ + doping(110 nm, wet-chemical processing)	Pt(50 nm)/Au(500 nm)	57 (1 GHz)	2.2	this work, ∇

Table 6.3 – The $Q_{\mathrm{intr}}(\eta(E_{\mathrm{bd}}))$ benchmark plot for BST MIM capacitors with data obtained from this work and from literature. The Q_{intr} together with its $\eta(E_{\mathrm{bd}})$ could not be retrieved from [40, 151], therefore the (total) Q is given with respectively the symbols 'X' and '+'.

Substrate	**Alumina**	**Silicon**
h	530 nm	110 nm
ε_r (1 MHz)	369 – 465	167 – 434
η (1 GHz)	3.2 – 4.0	1.3 – 4.7
C/A [nF/mm^2] (1 MHz)	6.3 – 7.9	13.3 – 29
Q (1 GHz)	30 – 22	76 – 39
Q_{intr} (1 GHz)	31 – 24	98 – 47

Table 6.4 – Summary of the obtained measurement results on alumina and silicon for the most important samples in this work. The bottom electrode on alumina consisted of Ti/Pt and on Si of both Ti/Pt as well as TiO_2/Pt.

Thin film BST MIM capacitors on alumina at 1 GHz in this work showed a Q_{intr} between 24–31, and tuning ratios between 3.1–4.0 (limited by the measurement equipment up to 40 V_{dc}). On silicon substrates at 1 GHz the Q_{intr} ranged between 47–125, and tuning ratios between 1.3–4.7.

A summary on the performance of this work is given in Table 6.4.

The $Q(\eta)$ data points in this work are presented by squared and triangular symbols in Table 6.3 and Figure 6.19, capacitors with relatively high tuning ratios between 1.3–4.7 were measured, with respectively Q_{intr} of 98–47 at 1 GHz. The interplay between the Q, Q_{intr} and η confirm the results of the literature survey in Section 2.

On the 530 nm thick BST films on alumina with $Ba_xSr_{1-x}Ti_{1.02}O_{3+z}$ with x = 0.8–1.0 and on 110 nm thick BST films on Si with x = 0.5–0.7 approximately the same maximum permittivities were measured (see Table 6.4), despite the much smaller dielectric thickness and less barium in the BST films on Si. The Q on silicon is higher in any case than on alumina. The maximum η is higher on Si (with a $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ composition).

Changes in the processing on silicon attributed to the performance by employing a different: 1) bottom electrode, 2) BST composition, and 3) substrate. Each modification is discussed below this point.

(1) the electrode configuration.
Experimental results in this work have shown that if BST is deposited on a Ti/Pt, instead of a TiO_2/Pt, bottom electrode a low-κ TiO_2 interface layer was present above the bottom electrode.
The relative permittivity decreases due to the interface layer with a lower dielectric constant, e.g., 70–80 for TiO_2 [147, 148], and with a bulk relative permittivity of the BST layer of typically $\gg 500$ in series.

The alumina samples are less sensitive to the TiO_2 interface layer due to the thicker dielectric layer. That finding is supported by Figure 6.3.

To eliminate the Ti interdiffusion through the Pt and the dead interface layer in BST, BST on silicon was processed with a TiO_2 layer below a 200 nm Pt bottom electrode, instead of a Ti layer below a 150 nm thick Pt bottom electrode, on silicon substrates. The electrical characterization showed an increase in tuning ratio with the TiO_2/Pt bottom electrode by more than a factor of 2.
The Pt bottom electrode thickness was increased to further suppress a possible Ti diffusion and to reduce the loss tangent. Additionally, the sheet resistance of the electrodes was reduced by adding a Au layer on top or an additional Au/Pt electrode on the Ti/Pt bottom (see Figures 4.11, 4.12, and 4.13).

The material and electrical characterization showed that the electrode configuration is crucial to obtain a high Q at RF, and to reduce the TiO_2 interface layer, so that the measured η increases for thin layers of BST.

(2) a change in BST composition.
This work shows that the Q increases ($\tan\delta$ decreases) at RF for a lower Ba content in barium strontium titanate solid solutions, as well as for a cation doping in BST. In bulk single crystalline ferroelectrics, the losses are highest next to the paraelectric-and-ferroelectric phase transition (see Chapter 3). The same trend is found in thin films, although the phase transition is smeared out and a broad maximum of the ε_r is found (see Figure 6.4).

Electrical measurements have shown that a lower Ba content in the solid BST solution or other cation doping in BST can decrease the Curie temperature below room temperature, which will reduce the losses.

The literature study in Section 2 and the measurements in this Chapter show that the BST composition can be tailored to the requirements of the application: a high Q at the cost of η or vice versa.

A compositional study with extensive material and electrical characterization on alumina has been submitted to Thin Solid Films [109].

(3) the grain size.

The annealing temperature of the dielectric layer influences the grain size in the dielectric, and affects the temperature dependence of the relative permittivity. G. Arlt et al. [82] made $BaTiO_3$ ceramics at various annealing temperatures, and demonstrated that the ε_r increases with grain size showing a maximum ε_r at room temperature up to 700 nm.
Measurements carried out by J.F. Ihlefeld et al. [84] on $BaTiO_3$ films, deposited by chemical solution deposition and annealed between 700–900 °C, shows that the grain size and ε_r increases with annealing temperature.
The data reported in [84] show that barium titanate ceramics and thin films with small grain sizes < 700 nm result in capacitors with reduced relative permittivities and reduced temperature dependence of the relative permittivity.
The grain size can be influenced not only by the annealing or post-annealing temperature, but also by the composition.

The material analysis results in this work in Table 6.2 show that a higher Ba content in the BST solid solution slightly increases average grain size. Therefore, the measured maximum ε_r increases (see Figure 6.4). Identical measurement observations were encountered by J.F. Ihlefeld et al. [84] and by I.P. Koutsaroff et al. [145].
The sensitivity of the ε_r against operation temperature of the *fine-grained thin* BST films showed a broad Curie maximum, i.e., a relatively constant ε_r (see Figures 6.4 and 6.6), which is beneficial for integration in reconfigurable RF circuits.

(4) substrate type.
The measurement techniques used on the samples on alumina and silicon were the same.

The substrate affects the Q as addressed in Section 6.1. Ideally the substrate would be a perfect insulator, eliminating the current flow through and the dissipated RF power in the substrate. However, since the homogeneous bottom electrode of our test structures shield the substrate, we expect very little RF signal leakage in the substrate to occur. Therefore, the parasitic capacitance is also very low.

The mismatch between the coefficient of thermal expansion (CTE) of the dielectric and that of the substrate affects the stress in the films

and in this way also the electrical properties of the films. T.R. Taylor et al. [152] compared the ε_r of BST on silicon and on sapphire and measured a difference of 6 %.
For the application and mass production, where the silicon substrate is one of the relevant substrates, the effect on the electrical properties will especially be determined by the electrodes (see Figures 4.11, 4.12, and 4.13) and the interface layers (see Figure 6.16).

6.7 Conclusions

Thin poly-crystalline barium strontium titanate films were deposited using wet chemical processing on poly-crystalline Al_2O_3 and single crystalline silicon substrates. High density MIM capacitor test structures for low and high frequency measurements were designed, realized and measured. With the obtained measurements and literature data a refinement of the process flow was done.
To optimized the flow reliable measurement data were required for the Q, Q_{intr}, ε_r and η. The measurement results are based on the measurement tools and techniques addressed in Chapter 4, which were employed to gain a better understanding on how improvements of the RF performance could be obtained.

The experiments showed that a higher barium content in BST films resulted in an increase of $T(\varepsilon_{r,\max})$ and grain size, which increased the relative permittivity, and hence a higher tuning ratio at the cost of the quality factor. Improvements of the electrodes were made by: 1) incorporating a TiO_2 layer below the bottom electrode, which showed an increase in η, and 2) by increasing the thickness of the metal electrodes with additional Pt or an Au/Pt layer, to reduce the loss tangent at RF and to form a barrier to prevent possible Ti diffusion through the bottom electrode into the BST.

Ferroelectric capacitors with a signal pad area as low as $50\,\mu m^2$ were processed and measured on alumina and silicon, yielding a good electrical performance. In this work, the parameters Q, Q_{intr} and η of ferroelectric capacitors, on alumina and silicon substrates, were assessed at radio frequencies, as key figures of merit. A trade-off between the quality of solely the dielectric Q_{intr} and tuning ratio η was found with $Q_{\text{intr}} = 100$ at $\eta = 1.2$, and $Q_{\text{intr}} = 47$ at $\eta = 4.7$.

Micro-and electrical characterization are crucial in obtaining insight in the quality of the layers of the ferroelectric capacitors. The outcome of the measurement results indicated where improvements could be made and supported the decision making on how to achieve a ferroelectric capacitor with a higher quality factor or tuning ratio. The applications and related specifications determine the demand on either the Q or η during process optimization.

The state of the art Q or η performance of our ferroelectric capacitors brings me to the conclusion that our ferroelectric capacitors can be considered for adaptive matching circuits.

Chapter 7

Model of a ferroelectric capacitor in a circuit simulator

7.1 Introduction

To simulate and design test circuits for tunable RF front-end applications, a ferroelectric capacitor component is required in the library of the circuit simulator. Agilent's Advanced Design System (ADS) circuit simulation software [153] has a state-of-the art library of microwave components and is therefore suited for circuit design like RF front-ends. However, a ferroelectric capacitor component is not part of the library. Therefore, a ferroelectric capacitor component has been implemented as a (tunable) building block in ADS and placed into the library.

The measured equivalent circuit in Figure 4.2 is used for the model in this Chapter.

For $C_{\mathrm{s}}(V_{\mathrm{dc}})$ an analytical description of the dielectric response from literature was employed. This model is valid in the paraelectric phase, where the capacitance response to the voltage does not depend on history. The model is therefore quasi-static and is valid for arbitrary voltage signals.

This model has been extended to include a bias shift. Then, the model parameters were fit to obtain a good agreement with measured $C(V_{\mathrm{dc}})$ results. Afterwards, the electrode resistance and losses are included in the model. Finally, the model has been implemented in ADS.

7.2 Model description of $C_{\mathrm{s}}(V_{\mathrm{dc}})$

The model of a parallel plate ferroelectric capacitor is based on a publication of O.G. Vendik and S.P. Zubko [154]. It features phenomenological adaptations to fit the thin-film data, and describes the voltage dependence of the capacitance in the paraelectric phase.

The voltage dependence of the capacitance, as given by [154], is rewritten as

$$C_{\mathrm{m}}(V) = \frac{C_{\mathrm{m}}(0)p_4}{(\sqrt{z^2+1}+z)^{\frac{2}{3}} + (\sqrt{z^2+1}-z)^{\frac{2}{3}} - 1} \tag{7.1}$$

with

$$z = \sqrt{(p_2(V+p_3))^2 + p_1}. \tag{7.2}$$

p_1–p_4 are voltage-independent fit parameters. The connection to the original parameters in [154] is given in Table 7.1. The parameter p3 on the other hand was additionally incorporated to the original model of [154].

Fit parameters
$p_1 = (\varsigma^{-3/4} \cdot \xi_{\mathrm{str}})^2$
$p_2 = (\varsigma^{3/4} h E_{\mathrm{N}})^{-1}$
$p_3 = \text{-}V_{\mathrm{shift}}$
$p_4 = \varsigma^{-1}$

Table 7.1 – The model fit parameters p_1–p_4.

p_1 is a shape parameter that is influenced by a temperature dependent parameter ς (see [154]; the symbol η in equation 7 is replaced by ς to avoid confusion with the definition of the tuning ratio) and a strain dispersion parameter ξ_{str} [154]. p_2 scales with the thickness of the dielectric layer h and the factor E_{N} normalizing electric field (see equation 15 in [154]). p_3 was added to the original model of [154], since the original model is mirror-symmetric around $V_{\mathrm{dc}} = 0\,\mathrm{V}$. p_3 models an internal bias voltage shift V_{shift} introduced by asymmetric processing of the electrodes or by different work

functions of the electrodes [46, 155, 156]. Finally, p_4 normalizes the function so that the capacitance at 0 V equals $C(0)$.

Note that only p_1 influences the shape of the $C_\mathrm{m}(V)$ curve. p_2-p_4 are just scaling and offset (shift) parameters.

The capacitance-voltage model, with the additional V_shift parameter (p_3), is validated in Figure 7.1 by fitting to $C(V_\mathrm{dc})$ measurement results of a realized 110 nm thick $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ MIM capacitor with $d = 16\,\mu$m on a silicon substrate.

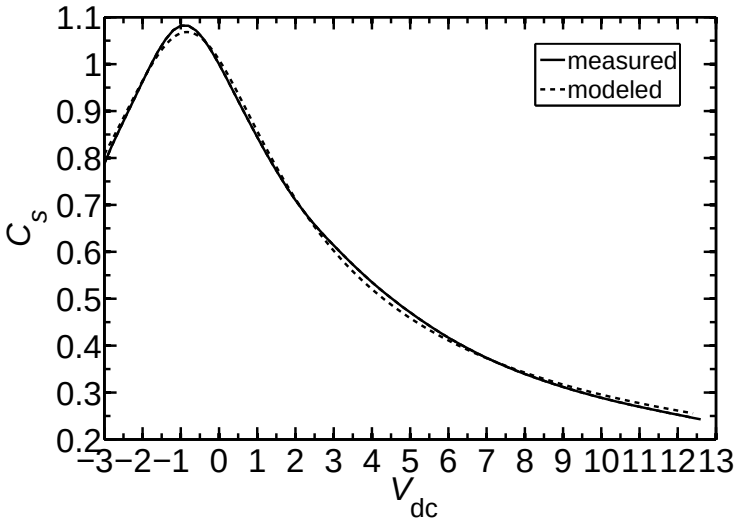


Figure 7.1 – Measurement results of a 110 nm $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$MIM capacitor with $d = 16\,\mu$m, on silicon at 0.9 GHz, and a fit of the ferroelectric capacitor model in ADS at room temperature, with the capacitance normalized at $0V_\mathrm{dc}$.

The model of the ferroelectric capacitor fits the measured capacitance well using equation 7.1. Only 4 fit parameter values were used with $p_1 = 1.78488$ $p_2 = 0.750345$, $p_3 = 0.840156$, and $p_4 = 1.66923$.

7.3 Model description of the losses

The dielectric and the electrodes contribute to the losses (see Section 4.2.5). The electrode resistance is modeled with a constant resistance value R_e, which can be calculated for certain geometries (see Section 4.2 for circular

capacitors), or needs to be simulated. The contribution from the dielectric is directly included as a fixed loss tangent in the ADS model. Currently, the model does not support a voltage dependence. The total loss can be calculated by equation 4.9.

Figure 7.2 shows a comparison between the measured and modeled loss tangent versus DC voltage at 0.9 GHz. For the model we used the extracted parameters from Chapter 4. The measured $\tan\delta_\varepsilon = 1/47$ at 1 GHz and $R_\mathrm{e} = 0.6\,\Omega$.

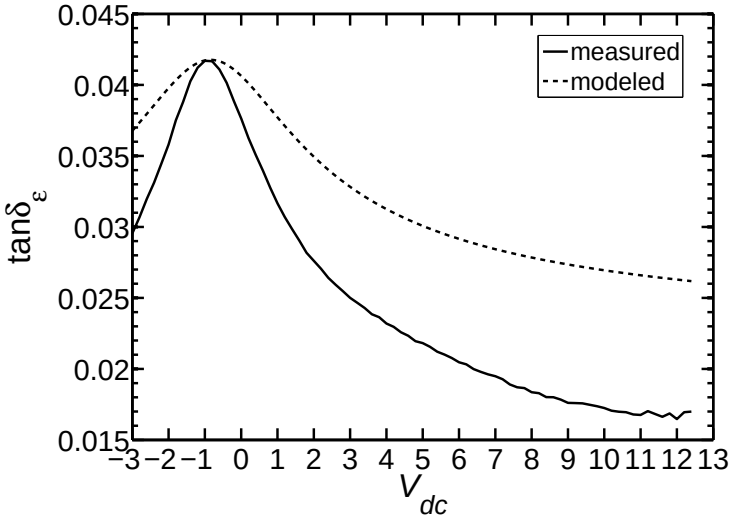


Figure 7.2 – Measurement results of the total $\tan\delta$ of the same capacitor as in Figure 7.1 and the model results are shown.

Figure 7.2 shows that a good fit was obtained at $0\,V_\mathrm{dc}$. This should be the case, since the loss tangent was extracted at $0\,V_\mathrm{dc}$. At higher voltages the dielectric loss is smaller than at zero volt. The total measurement loss deviate is lower than the modeled loss.

7.4 Model implementation in ADS

A non-linear capacitor is implemented by a Symbolically Defined Device (SDD) component in ADS, which uses currents and voltages. This component provides the highest flexibility.

Implicit or explicit non-linear equations [157] of the currents and voltages at the ports can be given. The current and voltages are connected by the impedance. The voltage is expressed as

$$V = ZI = \left(R_\mathrm{e} + R_\mathrm{d} + i\frac{-1}{\omega C_\mathrm{s}}\right) I = \left(R_\mathrm{e} + \frac{1}{i\omega C_\mathrm{s}}(i\tan\delta_\varepsilon + 1)\right) I \quad (7.3)$$

with Z as in equation 4.5 and R_d as in equation 4.3. R_e is implemented as a resistor in series 'Rseries' to the SDD component (see Figure 7.3). The remaining part of the impedance

$$\underbrace{i\omega}_{H_1}\ \underbrace{V_\mathrm{SDD}}_{f_1} + \underbrace{(1 + i\tan\delta_\varepsilon)}_{H_2}\ \underbrace{\frac{-I_\mathrm{SDD}}{C_\mathrm{s}}}_{f_2} = 0 \quad (7.4)$$

is implemented in the SDD component. Equation 7.4 is a small-signal equation in the frequency domain. However, if the same functions f_1 and f_2 are used in the time domain for the SDD model, then the model can be used for large signals as well (not derived here, see the ADS documentation for a lossless capacitor).

The SDD component uses internal Fourier-transformation F, so that it also can be used in the time and frequency domains. Firstly, the voltages and currents are transformed to the time domain. Then the user-defined non-linear functions f_k of voltages V_SDD and currents I_SDD are evaluated in the time domain. The results of f_k are transformed to the frequency domain and multiplied by a pre-defined or user-defined weighting factor H_k, which can be a function of frequency. The weight H_1 is pre-defined as $i\omega$. Finally, all components are summed and the model is iterated until the defining equation

$$\sum_\mathrm{k} H_\mathrm{k} F(f_\mathrm{k}) = 0 \quad (7.5)$$

converges to a solution in the frequency domain.

In Figure 7.3 the implementation is shown of the SDD component in series with a resistor, representing the electrodes. The schematic in ADS is converted to a new functional building block, which is placed in the local component library of ADS, representing a tunable ferroelectric capacitor component. The tunable ferroelectric capacitor model is useable in the major simulation modes (small signal in the frequency domain, large signal harmonic balance, and transient simulations in the time domain).

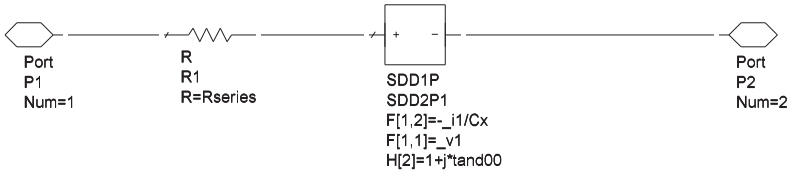


Figure 7.3 – A schematic of a 2-port ferroelectric capacitor modeled by a SDD component in combination with a resistor in ADS. At port 1 the current in ADS is represented by _i1 and the voltage by _v1. The Rseries in the schematic represent the electrode resistance R_e. The $\tan\delta 00$ in the schematic represents the $\tan\delta_\varepsilon$ (see equation 4.3). The weighting functions are presented as H[k] in ADS.

7.5 Discussion and conclusions

The model of a ferroelectric capacitor in the paraelectric phase at room temperature has been outlined. The capacitance within the model is constant with frequency. The implementation in ADS can describe a $C(V_{dc})$ measurement with only 4 fit parameters (p_1–p_4) of which p_2 and p_4 are 'trivial' scaling parameters. A single shape parameter p_1 already yields a very good fit to the measurements, when an appropriate voltage shift p_3 is applied.

A constant dielectric loss tangent is assumed, which is a fair assumption for the frequency dependence of the measured samples up to 8 GHz (see for example Figure 4.9). Furthermore, a ferroelectric capacitor, in an RF application, will most probably tune the frequency by less than a decade, which results in a deviation of the $\tan\delta_\varepsilon$ of less than +1 % (see e.g. Figure 4.9). This fits the ferroelectric capacitance response better than a model with a constant resistance (see Figure 2.3), and is therefore described by a single parameter.

The voltage dependence of the dielectric loss tangent shows a good fit close to zero volt. At higher voltages, the model overestimates the loss. The model can nevertheless be used for simulations of applications, as discussed in the next Chapter, to estimate the minimum quality factor.

The complete model requires 6 parameters: 4 for the $C_s(V_{dc})$ dependence, 1 for the dielectric loss tangent and 1 for the electrode resistance.

The novel ferroelectric capacitor component implementation in ADS can be integrated in electronic circuit simulations to investigate the effect of electri-

cal circuit tuning on the circuit performance. Examples will be elaborated and discussed in Chapter 8.

Chapter 8

Application of tunable capacitors in RF circuits - A simulation study

8.1 Introduction

In Chapter 7, a custom ferroelectric capacitor component was implemented and placed into the library of ADS. This component is embedded into two RF front-end applications. This facilitates the simulation of circuits employing this new component. In this chapter, two RF front end circuits are designed and simulated to assess the potential of the developed ferroelectric capacitors in cellular phone electronics.

The BST capacitor is inherently nonlinear for large signals, i.e. when the signal amplitude is significant compared to the maximum tuning voltage. The component must be realized such that harmonic distortion plays no significant role, e.g. by making the BST sufficiently thick. However, this chapter does not address harmonic distortion, but studies the basic feasibility of a tunable circuit using our component (assuming sufficient linearity can be obtained).

In Section 8.2, a transmit bandpass filter is designed and simulated with lossy linear capacitors and with the custom ferroelectric capacitor compo-

nent. Ferroelectric tunable filters using BST are known [111, 158–160], but are not yet used in cellular phones. The feasibility of fulfilling the insertion loss specifications of these test circuits with ferroelectric capacitors and inductors has been investigated.

In Section 8.3, an antenna impedance matching network is simulated with the custom ferroelectric capacitor component with measured component parameters. The improvement over not using a matching network is simulated in the case that a user places his or her hand on the antenna.

8.2 Transmit bandpass filter

Cellular phones can simultaneously send and transmit signals. This is achieved by separating the receive from the transmit frequencies. A duplex filter separates these signals from a single antenna. This chapter will discuss one half of a duplex filter, namely the transmit filter. It should have a low loss for the transmitted signal, but should block all signals at the receive frequencies. Otherwise, the receiver will be desensitized by the transmit signal.

A bandpass filter (BPF) has 1 passband and 2 stopbands. In the passband, the signal is attenuated as little as possible. The magnitude of the transmission S-parameter expressed in dB is called the insertion loss [161, 162]

$$IL(\text{dB}) = -20\log(|S_{21}|) = -10\log(|S_{21}|^2) \tag{8.1}$$

According to the Federal Standard 1037 Home [162], the insertion loss is defined as the reciprocal of the ratio of the signal power delivered to that part of the line following the device to the signal power delivered to that same part before insertion. The transmitted power relative to the available input power is $|S_{21}|^2$. Without a device the $S_{21} = 1$.
In the stopband, a strong attenuation of $S_{21,\text{stop}}$ is preferred for a BPF. The reflection parameter is expressed as S_{11} and should be low for a minimum insertion loss. Throughout this Chapter, the S-parameters are expressed in dB.

A typical transfer characteristic of a bandpass filter (BPF) is shown in Figure 8.1. The -3 dB passband bandwidth of a BPF is expressed, in equation

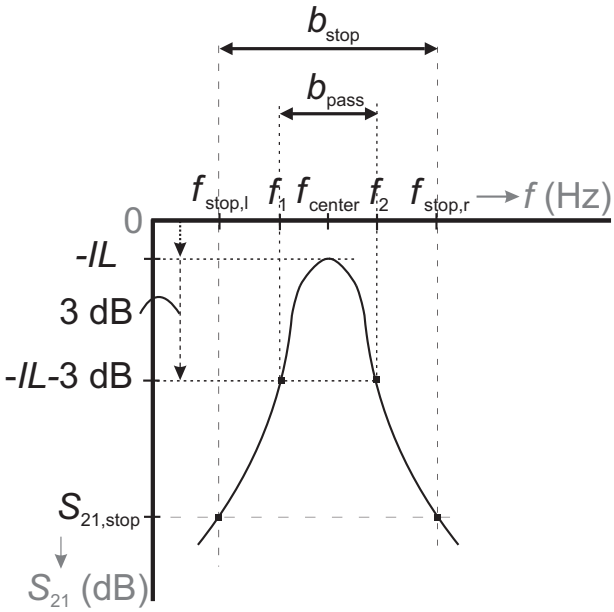


Figure 8.1 – The sketched S_{21} versus frequency of a single L-C-resonator.

11.07-01 in [163], as

$$b_{\text{pass}} = \frac{f_2 - f_1}{f_{\text{center}}} \tag{8.2}$$

(see Figure 8.1). At f_1 and f_2 the IL is 3 dB more than the minimum IL at the center frequency f_{center}.

The stopband attenuation $S_{21,\text{stop}}$ is specified at two frequencies. The left stopband frequency is denoted as $f_{\text{stop,l}}$ ($< f_{\text{center}}$) and the right stopband frequency as $f_{\text{stop,r}}$ ($> f_{\text{center}}$). The fractional stopband width is defined analogously to the passband width (see Figure 11.07-1 in [163]). When the right specification is closest to the f_{center} (see Table 8.1), then the stopband bandwidth is defined as

$$b_{\text{stop}} = 2\frac{f_{\text{stop,r}} - f_{\text{center}}}{f_{\text{center}}} \tag{8.3}$$

to fulfill the toughest stopband specification.

The specification of the cellular transmit filter for the S_{21} and S_{11} at the f_{center}, and the stopband attenuation $S_{21,\text{stop}}$ at specific frequencies on either side of the passband are given in Table 8.1.

Frequency f	S_{11}	S_{21}
$f_{\text{stop,l}} = 1.6\,\text{GHz}$ (stopband)	-	$<$ -20 dB
$f_{\text{center}} = 1.85\,\text{GHz}$ (passband)	$<$ -10 dB	$>$ -3 dB
$f_{\text{stop,r}} = 1.93\,\text{GHz}$ (stopband)	-	$<$ -25 dB

Table 8.1 – The minimum requirements of the tunable cellular transmit BPF, as provided by NXP.

The specifications show that the center frequency of 1.85 GHz is very close to the nearest stop-band frequency of 1.93 GHz. A narrow-bandpass filter design [163, 164] is required with a steep transition between the pass- and stopband. For narrow bandpass filter designs coupled resonator topologies are commonly employed [163, 165]. f_{center} is the resonance frequency of each isolated resonator. In all cases, the resonance frequencies for all resonators are identical.

The resonators are designed and simulated with lumped element inductors and capacitors. Lumped elements provide an adequate description of the circuit, because it is meant to be realized with physical dimensions much smaller than the wavelength of 1.85 GHz (16 cm), so that distributed effects can be neglected.

The angular frequency of an L-C resonator is

$$\omega_0 \;=\; 2\pi f_0 \;=\; 1/\sqrt{LC}\,. \tag{8.4}$$

If the capacitor C is used to tune the resonance frequency between 900 MHz and 1800 MHz, then the tuning ratio of the capacitor should be $\eta \geq 4$. This would cover the most common cellular bands. But also two filters with a smaller tuning range from 0.8–1 GHz or from 1.8–2 GHz would cover most frequency bands. This would require a capacitance tuning ratio of only $\eta \geq 1.5$. The sample measured in this work that reaches this η in Table 6.3 has a Q_{intr} of 67 at 1 GHz and 61 at 1.85 GHz.

The best available coils are air inductors and have a high quality factor of the inductor Q_L at RF [166]. A $Q_L = 220$ is feasible at $f = 1.85\,\text{GHz}$ for $L \leq 3.85\,\text{nH}$ [166]. Inductors are larger than ferroelectric capacitors. The number of inductors should therefore be minimized.

In the following paragraph relations are derived between the insertion loss and filter parameters, which will be used to determine the minimum amount

of resonators. Finally, the coupling between the resonator is further refined to reduce the number of inductors and to reduce the required quality factor of the components.

8.2.1 Relation between the insertion loss and filter parameters

To minimize the amount of capacitive tuning elements, the filter should have a minimum amount of resonators (i.e. filter order) and at the same time it should operate within the given specifications.

For a narrow bandpass filter response, the minimum insertion loss $IL_{\min}$ can be calculated for an arbitrary number of resonators. Using equation 8.3 in this chapter and equation 11.07-5 in [163] the minimum insertion loss becomes:

$$IL_{\min} = \frac{\frac{10\,\mathrm{dB}}{\ln 10} n_{\mathrm{r}} \exp\left(\frac{1}{n_{\mathrm{r}}}\left[\frac{-\ln 10}{20\,\mathrm{dB}} S_{21,\mathrm{stop}} + \ln 2\right]\right)}{b_{\mathrm{stop}} \cdot Q_{\mathrm{res}}}. \tag{8.5}$$

It depends on the stopband bandwidth b_{stop}, the quality factor of the resonator Q_{res} and the number of resonators n_{r}.

The optimum number of resonators required to fulfill the fixed stopband specification at b_{stop} can be derived by minimizing $IL_{\min}$

$$\frac{\mathrm{d}(IL_{\min})}{\mathrm{d}n_{\mathrm{r}}} = 0, \tag{8.6}$$

which yields the optimum number of resonators

$$n_{\mathrm{opt}} = \left(\frac{-\ln 10}{20\,\mathrm{dB}}\right) S_{21,\mathrm{stop}} + \ln 2\,. \tag{8.7}$$

Thus, to calculate n_{opt}, only the $S_{21,\mathrm{stop}}$ stopband specification is required. The optimum number of resonators, calculated using equation 8.7, has been confirmed by the data in Figure 11.07-2 in [163].

Equation 8.5 can now be rewritten as

$$IL_{\min} = \frac{\frac{-10\,\mathrm{dB}}{\ln 10} n_{\mathrm{r}} \exp\left(\frac{n_{\mathrm{opt}}}{n_{\mathrm{r}}}\right)}{b_{\mathrm{stop}} \cdot Q_{\mathrm{res}}}\,. \tag{8.8}$$

Finally, the minimum insertion loss for an optimum number of resonators is expressed as

$$IL_{\min}(n_{\mathrm{r}} = n_{\mathrm{opt}}) = \left(\frac{-1.4 \cdot S_{21,\mathrm{stop}} + 8.1\,\mathrm{dB}}{b_{\mathrm{stop}} \cdot Q_{\mathrm{res}}} \right). \tag{8.9}$$

This equation shows that the $IL_{\min}$ increases, when the stopband attenuation $S_{21,\mathrm{stop}}$ needs to be high or when the component quality factors are low. The closer the spacing between the pass- and stopband b_{stop}, the higher the $IL_{\min}$.

The optimum amount of resonators for a stopband attenuation $S_{21} = $-25 dB (see Table 8.1) is $n_{\mathrm{opt}} = 3.57$ and therefore requires 3 or 4 resonators. The S_{21} does not strongly depend on the number of resonators (see equation 8.8). Two, three and four resonators have respectively a 23 %, 1.6 % and 0.6 % higher IL relative to the $IL_{\min}(n_{\mathrm{r}} = n_{\mathrm{opt}})$. The advantage of using 4 resonators is therefore small.

To determine the Q_{res}, equation 8.8 is employed when $IL(f_{\mathrm{center}}) = $-3 dB (see Table 8.1). For $n = 2$, the Q_{res} of the resonators should be larger than 200 and for $n = 3$, the $Q_{\mathrm{res}} \geq 165$. Figure 8.2 shows the simulation results for the calculated values for 2 and 3 resonators. Both curves meet the specifications in Table 8.1 and confirm the simulations.

In this simulation L-C resonators were employed. The quality factor of an L-C resonator is determined by the inductor quality factor Q_L and the capacitor quality factor Q_C following

$$\frac{1}{Q_{\mathrm{res}}} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{8.10}$$

This means that the Q_L and Q_C must be higher than $Q_{\mathrm{res}} \geq 165$, which is currently not feasible.

The above calculations are for narrow BPFs where the stopband attenuation is high over a very broad stopband. However, in cellular applications the stopband attenuation is mainly needed in the receive band. This offers the opportunity to relax the stopband attenuation remote from 1.93 GHz.

In the following section, a technique is discussed to create a narrowband notch at the toughest stopband frequency of 1.93 GHz. The advantage is that the component quality factors can be lower. In addition, a lower number of resonators is desired to save area and, hence, cost. An IL is only

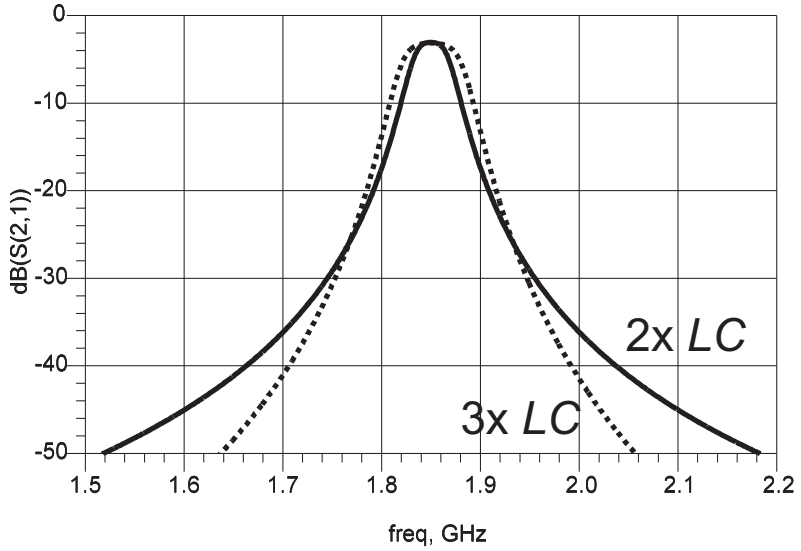


Figure 8.2 – The simulations of S_{21} (in dB) with 2 and 3 L-C resonators with respectively $Q_{\text{res}} = 200$ and $Q_{\text{res}} = 165$.

23 % higher than that of 3 resonators. In the following section, a case is therefore worked out for 2 resonators.

8.2.2 Capacitive or inductive coupling

Besides a higher Q_{res} to improve the stopband attenuation, frequency dependent coupling between the resonators can also increase the stopband attenuation. In the passband of the narrowband BPF a stronger coupling at f_{center}, and a weaker or zero coupling at $f_{\text{stop,r}}$ increases the attenuation in the stopband [165]. Therefore, Q_{res} can be reduced to reach the same IL. This can be realized by combined capacitive and inductive coupling or by cross-coupling between the resonators. In [167] an overview is given on how to implement capacitive and inductive coupling.

Capacitive and inductive coupling lead to different asymmetric frequency responses (see Figure 8.3). An inductive coupling allows frequencies below the passband to pass more easily and above the passband higher frequencies are further suppressed [165]. For a capacitive coupling it is vice versa [165]. Combined inductive and capacitive coupling can cancel each other and result

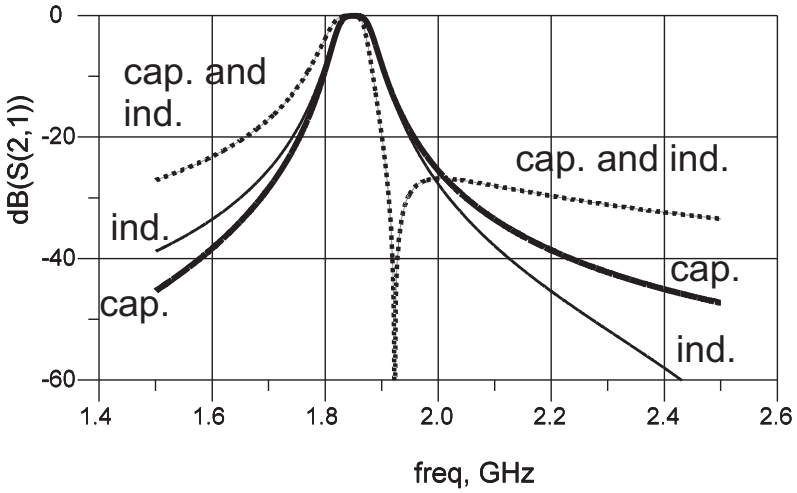


Figure 8.3 – The simulated influence of inductive coupling (ind.), capacitive coupling (cap.), and the combined capacitive and inductive coupling (cap. and ind.) on the S_{21} of a lossless BPF.

in a notch (strong local signal suppression) at the stopband, while (still) coupling in the passband remains [165]. The notch suppresses the signal in a small frequency band. The combined coupling results in less stopband attenuation far away from the notch (see Figure 8.3 and [165]).

The implementation of the coupling in the narrow BPF is described in the next paragraph.

8.2.3 Filter implementation in ADS

Narrow-band bandpass filters were designed and simulated in ADS using two parallel L-C resonators (see Figure 8.4) with a notch at the toughest stopband specification. Both resonators are identical and are terminated with $50\,\Omega$. C_{L1} and C_{L2} are input and output capacitors. $C_{\mathrm{p},1}$ and $C_{\mathrm{p},2}$ are the tunable capacitors. The capacitive coupling is implemented by C_{c} (see Figure 8.4). It forms a so called J-inverter (see [163] for more details). The inductive coupling is formed by a mutual coupling (see Figure 8.4) between the inductors or by an additional coupling inductor as shown in [167].

Scattering parameter sweeps have been performed from 1.5–2.5 GHz in steps of 1 MHz. The component values were varied until the stop-

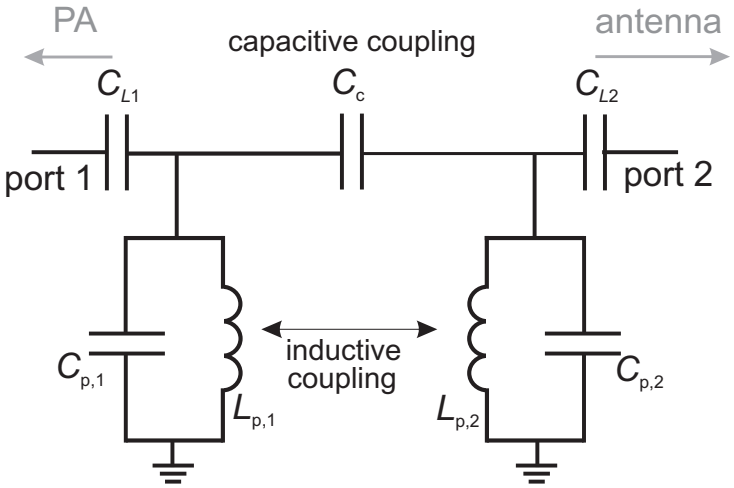


Figure 8.4 – The artist impression of the ADS schematic of the 2nd order narrowband BPF implementation.

band specifications were met. The inductive coupling factor equals 0.35. For the inductor, the present state of the art has a $Q_L = 220$ when $L_{p,1} = L_{p,2} = 2.5\,\text{nH}$ [166]. The other component values are $C_{p,1} = C_{p,2} = 1.46\,\text{pF}$ with $C_{coupling} = 0.55\,\text{pF}$ and $C_{L1} = C_{L2} = 0.35\,\text{pF}$.

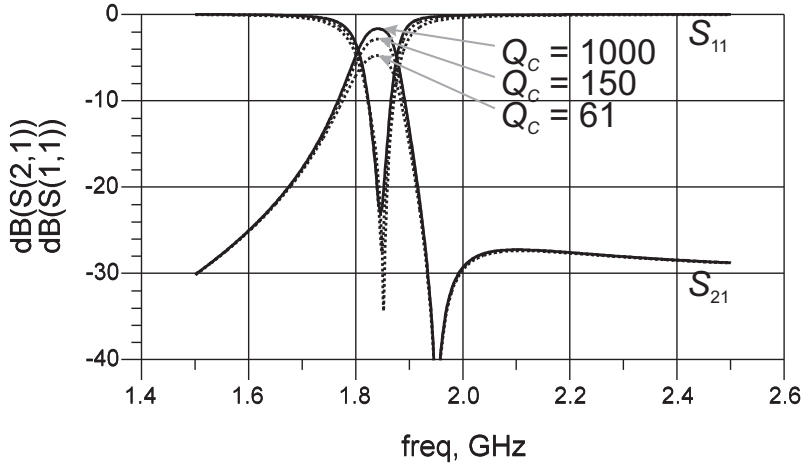


Figure 8.5 – The simulation results of the 2nd order BPF with a constant inductor quality factor and a quality factor for the capacitors of 1000, 150 and 61.

Figure 8.5 shows the influence of the quality factor of the tunable capacitors. Simulations have been performed with quality factor of 1000, 150 and 61. The latter represents the measured quality factor for the $Ba_{0.5}Sr_{0.5}Ti_{1.02}O_{3+z}$ sample at 1.85 GHz in this work. The results show that the specifications are fulfilled for a quality factor of 150 or higher for the capacitors. The Q_{res} then becomes 89 using equation 8.10. With a $Q_{\text{C}} = 61$, Q_{res} is equal to 48 and is therefore too low. The filter design is such that the capacitor value is only a few pF and the influence of the electrode resistance becomes small and can be lowered further by thick metals. Therefore, the intrinsic quality factor is the most dominant part of the total quality factor.

At this moment in time the required unloaded quality factors are not feasible for ferroelectric capacitors (see Figure 6.19) with a tuning ratio of $\eta > 2$. One of the major issues is the 80 MHz small spacing between the transmit and receive bands, which mandates a high quality factor for the components.

Impedance matching networks in the RF front-end do not have this strict requirement of 80 MHz spacing separation between the pass- and stopband. Therefore, it can be expected that the quality factor for the components can be lower. In the following section, the required quality factors are investigated for impedance matching networks.

8.3 Impedance matching networks

The second studied ferroelectric capacitors is an adaptive antenna impedance matching network. The purpose of an impedance matching network (IMN) is to have an optimal power flow from the source to the load to avoid reflections. Preferably, the load has to absorb all of the power transmitted from the source. To achieve this, the source impedance must be equal to the conjugate of the (complex) load impedance.

The impedance of an antenna is sensitive to environmental changes and always becomes complex by, e.g., holding a cellular phone to the ear of the user [4, 168–170]. To eliminate the imaginary part of the load, to obtain the characteristic impedance of 50 Ω, the matching network should have an output impedance which equals the conjugate of the antenna impedance. Tunable capacitors can re-tune the circuits impedance towards or to the characteristic impedance Z_0 [71, 171].

The potential of (continuously tunable) ferroelectric capacitors in impedance matching networks was studied by using the measured quality factor at $f = 1\,\text{GHz}$ from this work (see Table 6.3). The aim is to design an RF tunable *L*-*C* impedance matching network using the custom ferroelectric capacitor component, as discussed in Chapter 7 with lossy components.

8.3.1 Definitions of Terms

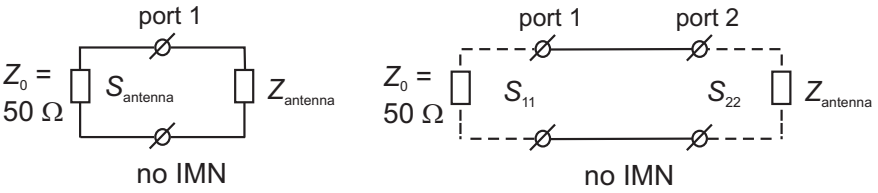


Figure 8.6 – An artist impression of a two-port network without an IMN.

Without an IMN [172] (see Figure 8.6), a part of the signal is reflected. The antenna reflection coefficient is calculated as

$$S_{\text{antenna}} = \frac{Z_{\text{antenna}} - Z_0}{Z_{\text{antenna}} + Z_0}. \tag{8.11}$$

A lossless network is inserted in Figure 8.6 to compare this with a matching network (see Figure 8.7). With a $50\,\Omega$ antenna the lossless network of Figure 8.6 will transfer all signals. The transmission parameters when the port impedance is normalized to Z_{antenna} are then $S_{11} = S_{22} = S_{\text{antenna}}$ and the transmission coefficient S_{21} is given by

$$|S_{21}| = \sqrt{1 - |S_{11}|^2} \tag{8.12}$$

since no energy is lost in the transfer network.

In Figure 8.7 an IMN is inserted. The antenna impedance is matched if the output impedance of the matching network (port 2) is the conjugate of the antenna impedance [172]. This means that the $50\,\Omega$ normalized antenna reflection coefficient S_{antenna} is also the conjugate of the $50\,\Omega$ normalized S_{22} parameter of the IMN.

In the following, the scattering parameters are normally given normalized to the antenna impedance. They then directly quantify the signal strength that is transferred to the antenna. An exception are calculations of the

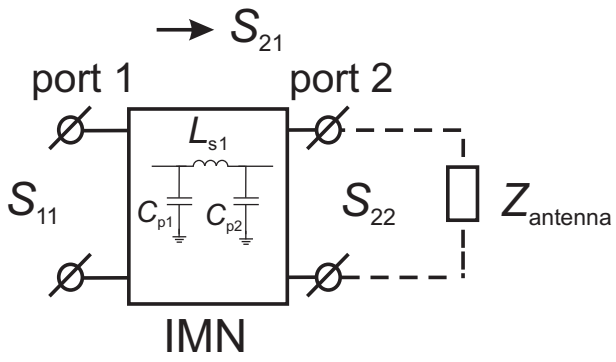


Figure 8.7 – An artist impression of a two-port lossless network with an IMN.

range of impedances that could be matched (in Smith Charts). Then a 50 Ω termination is more suited for the plots and simulations.

The design of the IMN is based on functional requirements and practical considerations, which will be discussed in the next paragraph.

8.3.2 Functional requirements and practical considerations

The impedance should be tuned back to the characteristic impedance, when a user interaction occurs. A study by T. Huang and K.R. Boyle [170] shows that placing a users hand on the antenna of a cellular phone, results in strong change in the antenna impedance from 50 Ω to $(14 + 60i\,\Omega)$, which implies a S_{21} = -4.5 dB. In other words, only 35 % of the power is transferred into the antenna.

This means that the battery will be drained faster. To maintain the same quality during the phone conversation additional power is required. It also means that received signals are weaker. A gain of 3 dB (factor 2 in power) would be a significant improvement. On the other hand, the transmission for a 50 Ω antenna should be still good. An additional IL of 1 dB implies that 21 % of the transmit power is dissipated in the IMN. That seems to be acceptable.

The topology of the impedance matching network (IMN) should preferably support:

- a tuning of the real and imaginary part of the output impedance.

- a minimum amount of inductors because of the large area consumption. The total inductance should be as low as possible.
- the elimination of unwanted signals at higher frequencies.
- the incorporation of parasitics in the topology as much as possible.
- blocking of the DC tuning voltage to the input and output ports.

8.3.3 Impedance matching networks topologies

There are various L-C low-pass and high-pass impedance matching network topologies. In IMN, the inductor and capacitor components are alternately placed to get a low- or high-pass behavior, or a combination of both to obtain a bandpass response. L-, T-, or Π-shape designs (see, e.g., [7, 42, 113, 163, 172, 173]), depicted in Figure 8.8, are the most commonly used topologies.

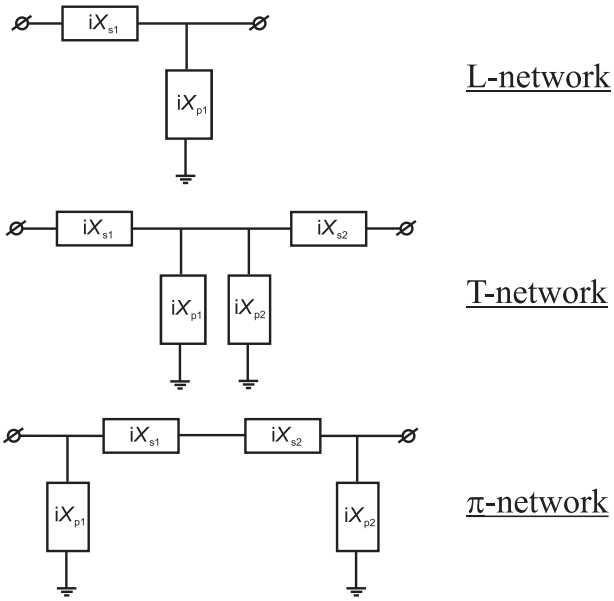


Figure 8.8 – Three single stage design topologies of filters with an alternating series reactance X_s and parallel reactance X_p of the inductors or capacitors.

An L-shape design with a series inductor in the schematic act as low-pass filter, and the networks with a series capacitor act as a high-pass filter.

Component values	Low-pass Π	High-pass Π	Low-pass T	High-pass T
$L_{\mathrm{ser},1}$	3.1 nH		39.8 nH	
$L_{\mathrm{ser},2}$			39.8 nH	
$L_{\mathrm{par},1}$		1.6 nH		20.7 nH
$L_{\mathrm{par},2}$		1.6 nH		
$C_{\mathrm{ser},1}$		8.3 pF		0.6 pF
$C_{\mathrm{ser},2}$				0.6 pF
$C_{\mathrm{par},1}$	15.9 pF		1.2 pF	
$C_{\mathrm{par},2}$	15.9 pF			

Table 8.2 – The component values of low-and high-pass Π- and T-matching networks at $Q_{\mathrm{loaded}} = 5$ at 1 GHz.

The addition of one more L-section to an L-section matching circuit results in a T- or a Π-section (see Figure 8.8). The T-shaped network is actually a back-to-back L-shaped network and a Π-shaped network consists also of two connected L-networks. Therefore, the first L-section has a different load now.

Different topologies require different component values. For a comparison the component values were calculated for the low-and high-pass L-C matching circuits of T- [7, 174] and Π-networks [173] $Q_{\mathrm{loaded}} = 5$ at 1 GHz with lumped ideal components (see Table 8.2). The loaded quality factor Q_{loaded} is a measure of how much the output impedance can be tuned (see e.g. [163] for more information).

The single Π-section topology has acceptable capacitance values and reasonably low inductance values. The single T-section topology has lower capacitance values and much larger inductance values. The high-pass Π and the low-pass T-matching networks require two inductors, while the remaining topologies require only one.

Taking the functional requirements and the practical considerations into account, and the data summarized in Table 8.2, the preferred topology is a low-pass Π-network. A low-pass Π-network has only one inductor with a low inductance value, the capacitance values easily realized in our technology, the parallel parasitic capacitances from the inductor can be absorbed and corrected for by ferroelectric capacitors (connected in parallel), and unwanted signals higher than the passband frequencies are eliminated automatically for a low-pass network.
The DC blocking can be achieved in all topologies by a series connection

of capacitors. The DC feed is connected at the center-tap in-between the capacitors in series (see Figure 8.9).

8.3.4 Impedance matching network implementations

In practice, besides parasitics, losses are present because of dissipation in the inductor and capacitors, bias resistors, and interconnects. Air inductors have a high Q at RF ($Q_L = 220$ is feasible at $f = 1\,\text{GHz}$; if $L = 2.5\,\text{nH}$ [166], or when $L = 8.8\,\text{nH}$ a $Q_L = 140$ is feasible [166]. The series inductor is indicated as 'Ls' in Figure 8.9.
The ferroelectric capacitors with the highest measured tuning ratio were used in the design: $\eta = 4.7$ with $Q_{\text{intr}} = 47$ (see Table 6.3) and the model parameters determined in Chapter 7.
From preliminary measurement results on demonstrator wafers with thicker electrodes a lower total series resistance of $0.2\,\Omega$ of the ferroelectric capacitors was measured for 20 pF capacitors. The bias resistors 'R2' and 'R3' (see Figure 8.9) were set at $5\,\text{k}\Omega$, which act as a DC feed to the capacitors. This value is more than 100 times higher than the capacitor reactance, thus resulting in less than 1 % loss through the bias resistor.

The schematic including lossy components is depicted in Figure 8.9.

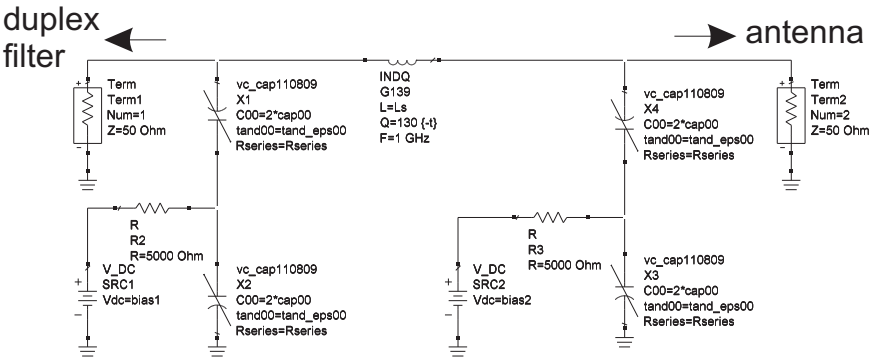


Figure 8.9 – The ADS schematic of the low-pass Π-IMN including the resistive loss of the bias-network and the dissipation of the inductors and capacitors. The parameter sweeps were performed at a single frequency point of 1 GHz. 'Rseries' represents the electrode resistance R_{e}. See the caption of Tables 8.3 and 8.4 for component values.

To investigate the hand interaction on the impedance of the antenna Z_{antenna} (Term2 in the ADS schematic) of the RF front-end, the impedance

of 63 users in Figure 6 of T. Huang and K.R. Boyle [170] was employed in the IMN design. The largest deviation from $50\,\Omega$ was measured in [170], when the hand is placed on the antenna, leading to $Z_{\text{antenna}} = (14 + 60i)\,\Omega$.

The series inductance value for a low-pass Π-network is calculated by [173]

$$L_{\text{s,lp}} = \frac{2R_{\text{input}}^2 C_{1,\text{par}}}{1 + (\omega R_{\text{input}} C_{1,\text{par}})^2} \tag{8.13}$$

and the loaded quality factor

$$Q_{\text{loaded}} = \omega R_{\text{input}} C_{1,\text{par}}. \tag{8.14}$$

The $C_{\text{par},1} = 21\,\text{pF}$ was determined after simulations, so that the Z_{antenna} can be matched. After calculation the inductance value $L_{\text{s,lp}} = 6.6\,\text{nH}$ and $Q_{\text{loaded}} = 2.64$. The unloaded quality factor of the inductors was set at a feasible $Q_{\text{u,inductor}} = 130$ [166].

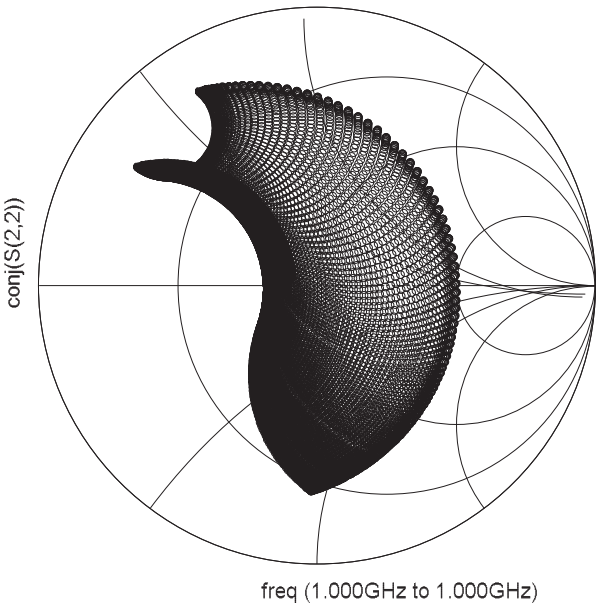


Figure 8.10 – The conjugate of the S_{22} of the matching network in Figure 8.9 is plotted in a Smith Chart at 1 GHz. The impedance of port 2 is $Z_{\text{antenna}} = 50\,\Omega$. See Table 8.3.

Total electrode resistance	loss without IMN		loss with IMN		+inductor on Term1 IMN	loss with IMN	
R_e (Ω)	S_{21} (dB)	S_{22} (dB)	S_{21} (dB)	S_{22} (dB)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)
0.05	0	-∞	-0.2	-20.2			
0.1	0	-∞	-0.3	-20.2	-0.52	-14.1	-16.7
0.2	0	-∞	-0.3	-20.2	-0.55	-14.0	-16.9
0.5	0	-∞	-0.3	-20.3			
1	0	-∞	-0.4	-20.3	-0.88	-12.4	-17.2

Table 8.3 – The effect of R_e of the ferroelectric capacitors on S_{21} and S_{22} at $Z_{antenna} = 50\,\Omega$ and $Z_{antenna} = 50\,\Omega$ with an additional series inductor connected to Term1. The results were obtained from ADS. Schematic parameter values: cap00 = 10.5 pF, L_s =6.6 nH and $Q_{loaded} = 2.64$.

Total electrode resistance	loss without IMN		loss with IMN		+inductor on Term1 IMN	loss with IMN	
R_e (Ω)	S_{21} (dB)	S_{22} (dB)	S_{21} (dB)	S_{22} (dB)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)
0.05	-4.5	-1.9	-2.3	-9.8			
0.1	-4.5	-1.9	-2.5	-9.8	-0.8	-22.1	-13.2
0.2	-4.5	-1.9	-3	-9.5	-0.9	-23.0	-12.9
0.5	-4.5	-1.9	-4.1	-8.6			
1	-4.5	-1.9	-5.4	-7.6	-1.5	-28.4	-11.2

Table 8.4 – The effect on R_e of the ferroelectric capacitors, the S_{21}, S_{11} and S_{22} at $Z_{antenna} = (14 + 60i)\,\Omega$ and $Z_{antenna} = (14+60i)\,\Omega$ with an additional series inductor connected to Term1. The results were obtained from ADS. Schematic parameter values: cap00 = 5.2 pF, L_s = 9.91 nH and $Q_{loaded} = 1.27$.

Figure 8.10 shows the simulation results in a Smith Chart [172]. A Smith Chart is a radial plot of the S-parameters. The conjugate of the S_{22} parameter is plotted, so that the Smith Chart directly shows the antenna impedance that could be matched. The Π-network can match inductive (upper half of the given Smith Chart) as well as capacitive loads (lower half of the given Smith Chart). It also can tune the resistive part.

Tables 8.3 and 8.4 list the S-parameters for the bias values at which the lowest insertion loss was found. The results in these tables show that if the input and output terminals are equal to 50 Ω, then S_{21} = 0 dB and S_{11} = -∞ dB, since all the power is absorbed in the (antenna) load without an IMN.
The addition of a matching network, when both ports are at 50 Ω, will slightly decrease the performance for S_{21} from 0 dB to -0.3 dB and for S_{22} from -∞ dB to -20.2 dB.

With an increasing R_e of the ferroelectric capacitors, the S_{21} increases due to more energy dissipation in the electrodes. The loss can be further decreased by adding an inductor, at the cost of a larger area, in series with the input port 1 (Term1). On the right side of Tables 8.3 and 8.4 the response is

shown.
The S_{21} improves from -4.5 dB (without a Π-IMN) to -3 dB (without a Π-IMN and an additional inductor at Term1) and to -0.9 dB (with a Π-IMN and an additional inductor at Term1) at $R_e = 0.2\,\Omega$, and the S_{22} from -1.9 dB (without a Π-IMN) to -9.5 dB (with a Π-IMN) and to -12.9 dB (with a Π-IMN and an additional inductor at Term1).

The simulation results have shown that the circuits with matching networks improve the S_{21} and S_{22} scattering parameters (at 1 GHz) significantly by more than 1 dB if the series resistance of the ferroelectric capacitors is $R_e \leq 0.2\,\Omega$. Then, the total Q of the ferroelectric capacitors with a $Q_{intr} = 47$ at $f_{center} = 1$ GHz, $R_e = 0.2\,\Omega$, C00 = 21 pF is approximately 20, which is considerably lower than for the filters.

8.4 Conclusions

The potential of ferroelectric capacitors in an RF front-end has been studied for a transmit bandpass filter and for an impedance matching network. The custom ferroelectric capacitor building block (as discussed in Chapter 7) was used for the ferroelectric capacitors in the design schematic. The parameter values were taken from measurements on ferroelectric capacitors with a high tuning ratio of 4.7 and a $Q_{intr} = 47$.

In a (tunable) filter with *L-C* resonators, the insertion loss is increased by increasing the number of resonators, the decrease in the quality factor of the components, and by a weaker coupling between the resonators. An expression was derived to determine the optimum number of resonators to acquire a minimum insertion loss, while still fulfilling the stopband specifications.

An optimum close to 3–4 resonators was calculated. However, to reduce the number of components (cost), the complexity and the size, two resonators were employed. The strict stopband specifications were met by utilizing capacitive and inductive coupling to create a notch in the stopband.

A 2nd narrowband tunable bandpass filter was designed and simulated in ADS. The customer specifications can be achieved, if the quality factor of the inductors and capacitors is higher than 150 and thus 75 for the parallel *L-C* resonator. Currently, these quality factors are not feasible employing thin film ferroelectric capacitors.

In addition, the potential of ferroelectric capacitors in an impedance matching network has been investigated. Lossy 2-port tunable IMNs with a low-pass Π-shape topology, one inductor, four ferroelectric capacitors and two bias resistors, were designed and simulated. Two independent DC bias sources were implemented for each parallel capacitor branch.

The performance improvement for a de-tuned antenna, taken from [170], was simulated for different electrode resistances. For a low-pass Π matching network an improvement of 1.5 dB is obtained for $R_e = 0.2\,\Omega$. Perfect electrodes would result in a significant improvement of circa 2.2 dB. An additional inductor at the input port leads to a major improvement of 3.6 dB. By using the matching network the power transmitted into the antenna is increased by a factor of over 2 for the de-tuned conditions. The matching will reduce the battery drain of the cellular phone.

For $R_e = 0.2\,\Omega$, the total quality of the capacitor including bias networks is around 20. It shows that the quality factor of currently available components are currently good enough for these networks.

In summary, the requirements of the transmit bandpass filter are currently too strict to be met with ferroelectric capacitors. Tunable impedance matching networks, using ferroelectric capacitors, show promising results for improving the circuits' performance. The impedance mismatch is significantly reduced using the low-pass Π-shape design topology.

Chapter 9

Conclusions

In this dissertation intensive electrical characterizations, modeling and the design of hardware with thin film barium strontium titanate (BST) tunable capacitors was carried out. Especially the quality factor Q and the tuning ratio η have been studied, since these are crucial parameters for reconfigurable RF front-end applications for mobile phones.

In a first step, the state of the art data for varactor diodes, dielectric varactors, semiconductor-switched capacitors, and micro machined electro mechanical systems was summarized from an intensive literature study (see Chapter 2). For all these devices, making use of the literature data, the relation between Q and η was described with basic physical models. The developed models for all the different devices could be combined into a new single formula that covers all technologies.

It could be derived for the different devices that:

- RF micro-electro-mechanical switches have the highest tuning potential with a high Q, but are large in size.
- For continuous, moderate tuning ranges $\eta < 3$, highly doped GaAs varactor diodes could offer the best performance.
- Dielectric varactors based on complex oxide layers will be most attractive for small physical size and low cost devices.

In a second step, RF tunable capacitors based on barium strontium titanate (BST) with an electrode area of $50\,\mu m^2$ or larger were designed, fabricated on alumina and silicon substrates, and measured. A dedicated analysis technique was developed to separate the electrical dissipation in the resistive electrodes from the dissipation in the dielectric oxide films (see Chapter 4). In order to prevent voltage-dependent impedance measurement errors, which occurred during RF $C(V_{dc})$ measurements with a commercial wide-band bias-tee, an additional open calibration was applied or measurements with a custom-made wide-band bias-tee were carried out (see Chapter 5).

The quality factor and tuning range were studied as a function of barium to strontium composition and doping in the BST films. A higher Q and a lower η was measured for a lower barium content in the BST films. Cation doping in the BST films can have a similar effect. At 1 GHz, a Q of 98 and a tuning ratio of 1.3 was determined for $Ba_{0.5}Sr_{0.5}Ti_{1.02}O_{3+z}$ films with doping. For $Ba_{0.7}Sr_{0.3}Ti_{1.02}O_{3+z}$ films, processed on top of TiO_2/Pt bottom electrodes quality factors of 47 and a tuning ratio of 4.7 was determined (see Chapter 6). The electrical characterization was utilized as an input to further improve the capacitors RF performance.

In a third step, a 2^{nd} order bandpass transmit filter and a low-pass Π-impedance matching network was designed and simulated in the design environment ADS, to obtain the requirements for ferroelectric capacitors (see Chapter 8). A ferroelectric capacitor model has been implemented as a new component (see Chapter 7). The model can describe a $C(V_{dc})$ measurement by only 4 fit parameters. The investigations show that for a bandpass transmit filter, a quality factor for the inductors and capacitors of at least 150 would be required.
The adaptive antenna impedance matching network was designed and simulated for a user, which covers the antenna with his hand, which results in a maximum impedance change from $50\,\Omega$ to $(14{+}60i)\,\Omega$. Tunable ferroelectric capacitors are promising for matching networks if the total Q at 1 GHz is above 20. In this case, the insertion loss could be improved from 4.5 dB without matching network, to 3 dB with a Π-matching network and to 0.6 dB with two cascaded low-pass L-sections.

The simulations and device characterization provided the link between the applications and the performance requirements of tunable capacitors. This is the basis to optimize the materials and devices for the applications.

Bibliography

[1] L. Besser and R. Gilmore, *Practical RF Circuit Design for Modern Wireless Systems*, vol. 1, Artech House Publishers, 2003.

[2] 2008, "Cellular Frequencies Standards", Available: http://www.etsi.org. See also http://www.itu.int.

[3] M. Helfenstein and G.S. Moschytz, Eds., *Circuits and Systems for Wireless Communications*, Kluwer Academic Publishers, 2002.

[4] D. Qiao, D. Choi, Y. Zhao, D. Kelly, T. Hung, D. Kimball, M. Li, and P. Asbeck, "Antenna Impedance Mismatch Measurement and Correction for Adaptive CDMA Transceivers", *IEEE MTT-S International Microwave Symposium Digest*, pp. 783–786, June 2005.

[5] Y. Tsividis, M. Banu, and J. Khoury, "Continuous-time MOSFET-C Filters in VLSI", *IEEE Transactions on Circuits and Systems*, vol. 33, no. 2, pp. 125–140, February 1986.

[6] N. Ning, X.P. Li, J. Fan, W.C. Ng, Y.P. Xu, X. Qian, and H.L. Seet, "A Tunable Magnetic Inductor", *IEEE Transactions on Magnetics*, vol. 42, no. 5, pp. 1585–1590, May 2006.

[7] I. Bahl, *Lumped Elements for RF and Microwave Circuits*, Artech House, 2003.

[8] M. Klee, D. Wissen, W. Keur, R. Kiewitt, D. Bausen, and P. Lok, "Oxide films for Integrated Capacitors in Thin Film Functional Modules", *Material Research Society*, vol. 655, pp. CC13.1.1–CC13.1.11, 2001.

[9] (2009), "The Philips Website. Online", Available: http://www.philips.com.

[10] (2009), "The NXP Semiconductors Website. Online", Available: http://www.nxp.com/.

[11] M.P.J. Tiggelman, K. Reimann, F. van Rijs, J. Schmitz, and R.J.E. Hueting, "On the Trade-off between Quality Factor and Tuning Ratio in Tunable High-frequency Capacitors", *IEEE Transactions on Electron Devices*, September 2009, [Accepted for publication].

[12] K.E. Mortenson, *Variable Capacitance Diodes: The operation and Characterization of Varactor, Charge Storage and PIN diodes for RF and Microwave Applications*, Artech, 1974.

[13] S.M. Sze and K.K. Ng, *Physics of Semiconductor Devices*, Wiley-Interscience, 3rd edition, October 2006.

[14] R.J. Soukup, "Capacitance of a Hyperabrupt Tuning Varactor Diode", *IEEE Transactions on Electron Devices*, vol. 23, no. 3, pp. 361–363, March 1976.

[15] C. Huang, L.C.N. de Vreede, F. Sarubbi, M. Popadic, K. Buisman, J. Qureshi, M. Marchetti, A. Akhnough, T.L.M. Scholtes, L.E. Larson, and L.K. Nanver, "Enabling Low-distortion Varactors for Adaptive Transmitters", *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 5, pp. 1149–1163, May 2008.

[16] K. Buisman, L.C.N. de Vreede, L.E. Larson, M. Spirito, A. Akhnoukh, Y. Lin, X. Liu, and L.K. Nanver, "Low-distortion, Low-loss Varactor-based Adaptive Matching Networks, Implemented in a Silicon-on-glass Technology", *IEEE Radio Frequency integrated Circuits (RFIC) Symposium*, pp. 389–392, June 2005.

[17] Meyer, R.G. and Stephens, M.L., "Distortion in Variable-capacitance Diodes", *Solid-State Circuits, IEEE Journal of*, vol. 10, no. 1, pp. 47–54, February 1975.

[18] G. Masetti, M. Severi, and S. Solmi, "Modeling of Carrier Mobility Against Carrier Concentration in Arsenic-, Phosphorus-, and Boron-Doped Silicon", *IEEE Transactions on Electron Devices*, vol. 30, no. 7, pp. 764–769, July 1983.

[19] W.D. van Noort, P. Deixler, R.J. Havens, and Angel Rodriguez, "Application of the 1-D Silicon Limit to Varactors", *IEEE Transactions on Electron Devices*, vol. 53, no. 7, pp. 1601–1607, July 2006.

[20] International Technology Roadmap for Semiconductors (ITRS), "Radio Frequency and Analog/Mixed Signal Technologies for Wireless Communications; Table RFAMS3b", Available: http://www.itrs.net Online, 2007.

[21] A.H. Meitzler, S. Trolier-McKinstry, J. Ballato, A. Bhalla, P. Bloomfield, W. Cao, L.E. Cross, J.P. Dougherty, J. Fousek, R. Guo, R.E. Newnham, S.M. Pilgrim, C.A. Randall, and Q. Zhang, "Draft 16 of A Working Document for a Proposed Standard to be entitled: IEEE Standard Definitions of Terms Associated with Ferroelectric and Related Materials", *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, vol. 50, no. 12, pp. 1613–1646, December 2003.

[22] R. Jakoby, P. Scheele, S. Muller, and C. Weil, "Nonlinear Dielectrics for Tunable Microwave Components", *IEEE Int. Conf. on Microwaves, Radar and Wireless Communications*, vol. 2, pp. 369–378, May 2004.

[23] A.K. Tagantsev, V.O. Sherman, K.F. Astafiev, J. Venkatesh, and N. Setter, "Ferroelectric Materials for Microwave Tunable Applications", *Journal of Electroceramics*, vol. 11, pp. 5–66, September 2003.

[24] W.P. Mason, "Electrostrictive Effect in Barium Titanate Ceramics", *Physical Review Letters*, vol. 74, no. 9, pp. 1134–1147, June 1948.

[25] Claeyssen, Colla, Cross, Damjanovic, Gaucher, Gevorgian, Gonnard, Lethiecq, Lubitz, Muralt, Safari, Schneider, Setter, Shrout, Trolier-McKinstry, Uchino, Wersing, Wolny, Yamashita, and co-authors, *Piezoelectric materials in devices*, 2002.

[26] J. Rosenbaum, *Bulk Acoustic Wave Theory and Devices*, Artech House, 1988.

[27] K.M. Lakin, G.R. Kline, and K.T. McCarron, "High-Q Microwave Acoustic Resonators and Filters", *IEEE Transaction on Microwave Theory and Techniques*, vol. 41, no. 12, pp. 2139–2146, December 1993.

[28] IEEE Standards Board, "IEEE Standard on Piezoelectricity", *IEEE*, January 1988.

[29] H.P. Loebl, C. Metzmacher, R.F. Milsom, P. Lok, F. van Straten, and A. Tuinhout, "RF Bulk Acoustic Wave Resonators and Filters", *Journal of Electroceramics*, vol. 12, no. 1–2, pp. 109–118, January 2004.

[30] M. Schreiter, R. Gabl, D. Pitzer, R. Primig, and W. Wersing, "Electro-acoustic Hysteresis Behaviour of PZT Thin Film Bulk Acoustic Resonators", *Journal of the European Ceramic Society*, vol. 24, pp. 1589–1592, September 2004.

[31] J. Berge, M. Norling, A. Vorobiev, and S. Gevorgian, "Field and Temperature Dependent Parameters of the DC Field Induced Resonances in $Ba_xSr_{1-x}TiO_3$-based Tunable Thin Film Bulk Acoustic Resonators", *Journal of Applied Physics*, vol. 103, pp. 064508, March 2008.

[32] A. Noeth, T. Yamada, V.O. Sherman, P. Muralt, A.K. Tagantsev, and N. Setter, "DC Bias-dependent Shift of the Resonance Frequencies in BST Thin Film Membranes", *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, vol. 54, no. 12, pp. 2487–2492, December 2007.

[33] S. Gevorgian, A. Vorobiev, and T. Lewin, "DC Field and Temperature Dependent Acoustic Resonances in Parallel-Plate Capacitors Based on $SrTiO_3$ and $Ba_{0.25}Sr_{0.75}TiO_3$ Films: Experiment and Modeling", *Journal of Applied Physics*, vol. 99, no. 124112, pp. 1–11, June 2006.

[34] IEEE Standards Board, "IEEE Standard Definitions of Primary Ferroelectric Terms", *IEEE*, June 1986.

[35] K.F. Astafiev, A.K. Tagantsev, and N. Setter, "Quasi-Debye Microwave Loss as an Intrinsic Limitation of Microwave Performance of Tunable Components Based on $SrTiO_3$ and $Ba_xSr_{1x}TiO_3$ Ferroelectrics", *Journal of Applied Physics*, vol. 97, no. 1, pp. 014106, December 2004.

[36] M.P.J. Tiggelman, K. Reimann, J. Liu, M. Klee, W. Keur, R. Mauczock, J. Schmitz and R.J.E. Hueting, "Identifying Dielectric and

Resistive Electrode Losses in High-density Capacitors at Radio Frequencies", *IEEE International Conference on Microelectronic Test Structures*, pp. 190–195, March 2008.

[37] A.K. Jonscher, "Dielectric Relaxation in Solids", *Journal of Physics D: Applied Physics*, vol. 32, no. 14, pp. R57–R70, July 1999.

[38] J.D. Baniecki et al., "Dielectric Relaxation of $Ba_{0.7}Sr_{0.3}TiO_3$ Thin Films from 1 MHz to 20 GHz", *Applied Physics Letters*, vol. 72, no. 4, pp. 498–500, January 1998.

[39] M. Schumacher and R. Waser, "Curie-Von Schweidler Behaviour Observed in Ferroelectric Thin Films and Comparison to Superparaelectric Thin Film Materials", *Integrated Ferroelectrics*, vol. 22, pp. 109–12109, March 1998.

[40] I.P. Koutsaroff et al., "Microwave Properties of Parallel Plate Capacitors Based on (Ba,Sr)TiO_3 Thin Films Grown on SiO_2/Al_2O_3 Substrates", *Materials Research Society*, vol. 784, no. C5.8, pp. 319–325, 2004.

[41] A. Vorobiev, P. Rundqvist, K. Khamchane, and S. Gevorgian, "Microwave Loss Mechanisms in $Ba_{0.25}Sr_{0.75}TiO_3$ Thin Film Varactors", *Journal of Applied Physics*, vol. 96, no. 8, pp. 4642–4649, October 2004.

[42] L.-Y. Vicki Chen, R. Forse, D. Chase, and R.A. York, "Analogue Tunable Matching Network using Integrated Thin-film BST Capacitors", *IEEE MTT-S International Microwave Symposium Digest*, vol. 1, pp. 261–264, June 2004.

[43] N.K. Pervez, P.J. Hansen, and R. York, "Optimization of High Tunability BST Thin Films Grown by RF Magnetron Sputtering", *IEEE Ultrasonics, Ferroelectrics, and Frequency Control*, pp. 278–280, August 2004.

[44] R.A. York, A.S. Nagra, P. Periaswamy, O. Auciello, S.K. Streiffer, and J. Im, "Synthesis and Characterization of $(Ba_xSr_{1-x})Ti_{1+y}O_{3+z}$ Thin Films and Integration into Microwave Varactors and Phase Shifters", *Integrated Ferroelectrics*, vol. 34, pp. 177–188, October 2001.

[45] T. Ayguavives, A. Tombak, J.-P. Maria, G.T. Stauf, C. Ragaglia, J. Roeder, A. Mortazawi, and A.I. Kingon, "Physical Properties of (Ba,Sr)TiO_3 Thin Films used for Integrated Capacitors in Microwave Applications", *IEEE International Symposium on Applications of Ferroelectrics*, vol. 1, pp. 365–368, 2000.

[46] O. Auciello, S. Saha, D.Y. Kaufman, S.K. Streiffer, W. Fan, B. Kabius, J. Im, and P. Baumann, "Science and Technology of High Dielectric Constant Thin Films and Materials Integration for Application to High Frequency Devices", *Journal of Electroceramics*, vol. 12, no. 1–2, pp. 119–131, January 2004.

[47] B.J. Laughlin, "Sputtered (Ba_x, Sr_{1-x})TiO_3, BST, Thin Films on Flexible Copper Foils for use as a Non-linear Dielectric", *Dissertation of the North Carolina State University, USA*, 2006.

[48] R. Schafranek, A. Giere, A.G. Balogh, T. Enza, Y. Zheng, P. Scheele, R. Jakoby, and A. Klein, "Influence of Sputter Deposition Parameters on the Properties of Tunable Barium Strontium Titanate Thin Films for Microwave Applications", *Journal of the European Ceramic Society*, vol. 29, no. 8, pp. 1433–1442, May 2009.

[49] R.L. Thayer, C.A. Randall, and S. Trolier-McKinstry, "Medium Permittivity Bismuth Zinc Niobate Thin Film Capacitors", *Journal of Applied Physics*, vol. 94, pp. 1941–1947, August 2003.

[50] J. Park, J.W. Lu, D.S. Boesch, S. Stemmer, and R.A. York, "Distributed Phase Shifter with Pyrochlore Bismuth Zinc Niobate Thin Films", *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 5, pp. 264–266, May 2006.

[51] D. Kelly, C. Brindle, C. Kemerling, and M. Stuber, "The state-of-the-art of silicon-on-sapphire CMOS RF switches", *IEEE Compound Semiconductor Integrated Circuit Symposium*, pp. 200–203, November 2005.

[52] S. Makioka, Y. Anda, K. Miyatsuji, and D. Ueda, "Super Self-Aligned GaAs RF Switch IC with 0.25 dB Extremely Low Insertion Loss for Mobile Communication Systems", *IEEE Transactions on Electron Devices*, vol. 48, no. 8, pp. 1510–1514, August 2001.

[53] P. Sjöblom and H. Sjöland, "Measured CMOS Switched High-Quality Capacitors in a Reconfigurable Matching Network", *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol. 54, no. 10, pp. 858–862, October 2007.

[54] K. Yamamoto, T. Heima, A. Furukawa, M. Ono, Y. Hashizume, H. Komurasaki, S. Maeda, H. Sato, and N. Kato, "A 2.4-GHz-band 1.8-V Operation Single-chip Si-CMOS T/R-MMICfront-end with a Low Insertion Loss Switch", *IEEE Journal of Solid-State Circuits*, vol. 36, no. 8, pp. 1186–1197, August 2001.

[55] T. McKay, M. Carroll, J. Costa, C. Iversen, D. Kerr, and Y. Remoundos, "Linear Cellular Antenna Switch for Higly-integrated SOI Front-end", *IEEE International SOI Conference Proceedings*, pp. 125–126, October 2007.

[56] J. Browne, "Enhanced UltraCMOS Yields GSM/CDMA switches", Available: http://www.mwrf.com Online; ED Online ID #11907, January 2006.

[57] F-J. Huang and K. O, "A 0.5-μm CMOS T/R Switch for 900-MHz Wireless Applications", *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 486–492, March 2001.

[58] J.M. Golio, *Microwave MESFETs and HEMTs*, Artech House Publishers, February 1991.

[59] G.M. Rebeiz, *RF MEMS – Theory, Design, and Technology*, Wiley & Sons, June 2002.

[60] J.J. Yao, "RF MEMS From a Device Perspective", *Journal of Micromechanics Microengineering*, vol. 10, pp. R9–R38, April 2000.

[61] H.D. Nguyen, D. Hah, P.R. Patterson, R. Chao, W. Piyawattanametha, E.K. Lau, and M.C. Wu, "Angular Vertical Comb-driven Tunable Capacitor with High-tuning Tunabilities", *Journal of Microelectromechanical Systems*, vol. 13, no. 13, pp. 406–413, June 2004.

[62] J-B. Yoon and C.T.-C. Nguyen, "A High-Q Tunable Micromechanical Capacitor with Movable Dielectric for RF Applications", *International Electron Devices Meeting (IEDM)*, pp. 489–492, December 2000.

[63] H. Lee, Y.J. Yoon, D-H. Choi, and J-B. Yoon, "High-Q, Tunable-gap MEMS Variable Capacitor Actuated with an Electrically Floating Plate", *IEEE International Conference on Micro Electro Mechanical Systems*, pp. 180–183, January 2008.

[64] Z.J. Yao, S. Chen, S. Eshelman, D. Denniston, and C. Goldsmith, "Micromachined Low-loss Microwave Switches", *IEEE Journal of Microelectromechanical Systems*, vol. 8, no. 2, pp. 129–134, June 1999.

[65] R.L. Borwick, P.A. Stupar, J. DeNatale, R. Anderson, C. Tsai, K. Garrett, and R. Erlandson, "A High Q, Large Tuning Range MEMS Capacitor for RF Filter Systems", *Sensors and Actuators A: Physical*, vol. 103, no. 1, pp. 33–41, January 2003.

[66] A. Dec and K. Suyama, "Micromachined Electro-Mechanically Tunable Capacitors and Their Applications to RF ICs", *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 12, pp. 2587–2596, December 1998.

[67] Th.G.S.M. Rijks, P.G. Steeneken, J.T.M. van Beek, M.J.E. Ulenaers, A. Jourdain, H.A.C. Tilmans, J. De Coster, and R. Puers, "Microelectromechanical Tunable Capacitors for Reconfigurable RF Architectures", *Journal of Micromechanics and Microengineering*, vol. 16, pp. 601–611, February 2006.

[68] Th.G.S.M. Rijks, J.T.M. van Beek, P.G. Steeneken, M.J.E. Ulenaers, J. De Coster, and R. Puers, "RF MEMS Tunable Capacitors with a Large Tuning Ratio", *IEEE International Conference on Micro Electro Mechanical Systems*, pp. 777–780, 2004.

[69] Teravicta Inc., "Datasheet TT12-68CSP-EB v2.2, SPDT 7 GHz Switch Connectorized Evaluation Board", Available: http://www.matweb.com/, July 2006.

[70] C. Goldsmith, J. Maciel, and J. McKillop, "Demonstrating Reliability", *IEEE Microwave Magazine*, vol. 8, no. 6, pp. 56–60, December 2007.

[71] A. v. Bezooijen, M. de Jongh, C. Chanlo, L. Ruijs, H.J. ten Dolle, P. Lok, F. van Straten, J. Sneep, R. Mahmoudi, and A.H.M. van Roermund, "RF-MEMS Based Adaptive Antenna Matching Module",

IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp. 573–576, June 2007.

[72] K. Buisman, C. Huang, A. Akhnoukh, M. Marchetti, L.C.N. de Vreede, L.E. Larson, and L.K. Nanver, "Varactor Topologies for RF Adaptivity with Improved Power Handling and Linearity", *IEEE MTT-S International Microwave Symposium Digest*, pp. 319–322, June 2007.

[73] J.-S. Fu, X.A. Zhu, D.-Y. Chen; J.D. Phillips, and A. Mortazawi, "A Linearity Improvement Technique for Thin-film Barium Strontium Titanate Capacitors", *IEEE MTT-S International Microwave Symposium Digest*, pp. 560–563, June 2006.

[74] C.K. Campbell, *Surface Acoustic Wave Devices for Mobile and Wireless Communications*, Academic Press, 1998.

[75] R. Strijbos, A. Jansman, J.-W. Lobeek, N.X. Li, and N. Pulsford, "Design and Characterisation of High-Q Solidly-Mounted Bulk Acoustic Wave Filters", *Proceedings of the Electronic Components and Technology Conference*, pp. 169–174, May 2007.

[76] G.N. Saddik, D.S. Boesch, S. Stemmer, and R.A. York, "DC Electric Field Tunable Bulk Acoustic Wave Solidly Mounted Resonator using $SrTiO_3$", *Applied Physics Letters*, vol. 91, no. 043501, July 2007.

[77] A. Volatier, E. Defaÿ, M. Aïd, A. N'hari, P. Ancey, and B. Dubus, "Switchable and Tunable Strontium Titanate Electrostrictive Bulk Acoustic Wave Resonator Integrated with a Bragg Mirror", *Applied Physics Letters*, vol. 92, no. 032906, January 2008.

[78] W. Pang, H. Zhang, H. Yu, C-Y. Lee, and E.S. Kim, "Electrical Frequency Tuning of Film Bulk Acoustic Resonator", *Journal of Microelectromechanical Systems*, vol. 16, no. 6, pp. 1303–1313, December 2007.

[79] J.C. Burfoot, *Ferroelectrics: An Introduction to the Physical Principles*, Van Nostrand, 1967.

[80] T. Sakudo and H. Unoki, "Dielectric Properties of $SrTiO_3$ at Low Temperatures", *Physical Review Letters*, vol. 26, no. 14, pp. 851–853, April 1971.

[81] K. Bethe, "Über das Mikrowellenverhalten Nichtlinearer Dielektrika", Tech. Rep. vol. 25, Philips Research, 1970.

[82] G. Arlt, D. Hennings, and G. de With, "Dielectric Properties of Fine-grained Barium Titanate Ceramics", *Journal of Applied Physics*, vol. 58, no. 4, pp. 1619–1625, August 1985.

[83] J.-P. Maria, C.B. Parker, A.I. Kingon, and G. Stauf, "Thickness, Strain, and Temperature-dependent Properties of Barium Strontium Titanate Thin Films", *IEEE International Symposium on Applications of Ferroelectrics*, pp. 151–154, May 2002.

[84] J.F. Ihlefeld, A.M. Vodnick, S.P. Baker, W.J. Borland, and J-P. Maria, "Extrinsic Scaling Effects on the Dielectric Response of Ferroelectric Thin Films", *Journal of Applied Physics*, vol. 103, no. 074112, pp. 1–6, April 2008.

[85] A.D. Hilton and B.W. Ricketts, "Dielectric Properties of $Ba_{1-x}Sr_xTiO_3$ Ceramics", *Journal of Physics D: Applied Physics*, vol. 29, no. 5, pp. 1321–1325, May 1996.

[86] C.B. Parker, J.-P. Maria, and A.I. Kingon, "Temperature and Thickness Dependent Permittivity of (Ba,Sr)TiO_3 Thin Films", *Applied Physics Letters*, vol. 81, no. 2, pp. 340–342, July 2002.

[87] B. Panda, A. Roy, A. Dhar, and S.K. Rayb, "Thickness and Temperature Dependent Electrical Characteristics of Crystalline $Ba_xSr_{1-x}TiO_3$ Thin Films", *Journal of Applied Physics*, vol. 101, no. 064116, pp. 1–7, March 2007.

[88] I.P. Koutsaroff, A. Kassam, M. Zelner, P. Woo, L. McNeil, T. Bernacki, A. Cervin-Lawry, and A. Patel, "Dielectric Properties of (Ba,Sr)TiO_3 Thin Film Capacitors Fabricated on Alumina Substrates", *Materials Research Society*, vol. 748, pp. U6.1.1–U6.1.10, December 2003.

[89] S. Ito, H. Funakubo, I.P. Koutsaroff, M. Zelner, and A. Cervin-Lawry, "Effect of the Strain from the Substrate on Tunability of (100) One-axis Oriented $(Ba_{0.5}Sr_{0.5})TiO_3$ Thin Films", *International Symposium on Applications of Ferroelectrics*, pp. 198–201, May 2007.

[90] T.M. Shaw, Z. Suo, M. Huang, E. Liniger, R.B. Laibowitz, and J.D. Baniecki, "The Effect of Stress on the Dielectric Properties of Barium Strontium Titanate Thin Films", *Applied Physics Letters*, vol. 75, no. 14, pp. 2129–2131, August 1999.

[91] N. Setter, D. Damjanovic, L. Eng, G. Fox, S. Gevorgian, S. Hong, A. Kingon, H. Kohlstedt, N.Y. Park, G.B. Stephenson, I. Stolitchnov, A.K. Taganstev, D.V. Taylor, T. Yamada, and S. Streiffer, "Ferroelectric Thin Films: Review of Materials, Properties, and Applications", *Journal of Applied Physics*, vol. 100, no. 051606, pp. 1–46, September 2006.

[92] Y. Fukuda, K. Numata, K. Aoki and A. Nishimura, "Origin of Dielectric Relaxation Observed for $Ba_{0.5}Sr_{0.5}TiO_3$ Thin-Film Capacitor", *Japanese Journal of Applied Physics*, vol. 35, no. 9B, pp. 5178–5180, September 1996.

[93] M.S.P. Lucas, "Distributed Effects in Thin-Film Capacitors", *Microelectronics and Reliability*, vol. 6, pp. 269–276, April 1967.

[94] E. Schrödinger, "Studien über Kinetik der Dielektrika, den Schmelzpunkt, Pyro- und Piezoelektrizität", *Sitzungsberichten der Kaiserl. Akademie der Wissenschaften in Wien. Mathem.-naturw. Klasse*, , no. Bd. CXXI. Abt.IIa, pp. 1–36, November 1912.

[95] J. Valasek, "Piezo-electric and Allied Phenomena in Rochelle Salt", *Physical Review*, vol. 15, pp. 537–538, 1920.

[96] J. Fousek, "Joseph Valasek and the Discovery of Ferroelectricity", *IEEE International Symposium on Applications of Ferroelectrics*, pp. 1–5, Augustus 1994.

[97] H. Mueller, "Properties of Rochelle Salt", *Physical Review*, vol. 47, pp. 175–191, 1935.

[98] H. Mueller, "Properties of Rochelle Salt", *Physical Review*, vol. 57, pp. 829–839, 1935.

[99] S. Roberts, "Dielectric and Piezoelectric Properties of Barium Titanate", *Physical Review Letters*, vol. 71, no. 12, pp. 890–895, March 1947.

[100] A.E. Feuersanger, A.K. Hagenlocher, and A.L. Solomon, "Preparation and Properties of Thin Barium Titanate Films", *Journal of the Electrochemical Society*, vol. 111, no. 12, pp. 1387–1391, December 1964.

[101] M. Klee, H. van Esch, W. Keur, B. Kumar, L. van Leuken-Peters, J. Liu, R. Mauczok, K. Neumann, K. Reimann, C. Renders, A.L. Roest, M.P.J. Tiggelman, M. de Wild, O. Wunnicke, and J. Zhao, "Ferroelectric Thin Film Capacitors and Piezoelectric Switches for Mobile Communication Applications", *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 56, no. 8, pp. 1505–1512, August 2009.

[102] A. Ioachim, M.I. Toacsan, M.G. Banciu, L. Nedelcu, C.A. Dutu, F. Sava, M. Popescu,N. Scarisoreanu, and M. Dinescu, "Characterization of $Ba_{0.5}Sr_{0.5}TiO_3$ Thin Films for Tuneable Devices", *International Semiconductor Conference*, vol. 2, pp. 271–274, September 2006.

[103] N.K. Pervez, P.J. Hansen, and R.A. York, "High Tunability Barium Strontium Titanate Thin Films for RF Circuit Applications", *Applied Physics Letters*, vol. 85, no. 19, pp. 4451–4453, November 2004.

[104] X. Liang, Z. Meng and W. Wu, "Effect of Accepter and Donor Dopants on the Dielectric and Tunable Properties of Barium Strontium Titanate", *Journal of American Ceramic Society*, vol. 87, no. 12, pp. 2218–2222, April 2004.

[105] J. Gong, J. Cheng, W. Zhu, S. Yu, W. Wu, and Z. Meng, "Improvement in Dielectric and Tunable Properties of Fe-doped $Ba_{0.6}Sr_{0.4}TiO_3$ Thin Films Grown by Pulsed-laser Deposition", *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, vol. 54, no. 12, pp. 2579–2582, December 2007.

[106] S.K. Streiffer, C. Basceri, C.B. Parker, S.E. Lash, and A.I. Kingon, "Ferroelectricity in Thin Films: The Dielectric Response of Fiber-textured $(Ba_xSr_{1-x})Ti_{1+y}O_{3+z}$", *Journal of Applied Physics*, vol. 86, no. 8, pp. 4565–4575, October 1999.

[107] V.M. Mukhortov, Yu.I. Golovko, Vl.M. Mukhortov and V.P. Dudkevich, "Characteristics of Growth of Complex Ferroelectric Oxide

Films by Plasma-ion Sputtering", *Russian Physics Journal*, vol. 24, no. 2, pp. 102–106, February 1981.

[108] C.J. Johnson, "Some Dielectric and Electro-optic Properties of $BaTiO_3$ Single Crystals", *Applied Physics Letters*, vol. 7, no. 8, pp. 221–223, October 1965.

[109] M.P.J. Tiggelman, K. Reimann, M. Klee, R. Mauczock, W. Keur, and R.J.E. Hueting, "$Ba_xSr_{1-x}Ti_{1.02}O_3$ Metal-Insulator-Metal Capacitors on Planarized Alumina Substrates", *Thin Solid Films*, 2009, [Accepted for publication].

[110] J. Nath, W.M. Fathelbab, P.G. Lam, D. Ghosh, S. Aygn, K.G. Gard, J.-P. Maria, A.I. Kingon, and M.B. Steer, "Discrete Barium Strontium Titanate (BST) Thin-Film Interdigital Varactors on Alumina: Design, Fabrication, Characterization, and Applications", *IEEE MTT-S International Microwave Symposium Digest*, pp. 552–555, June 2006.

[111] A. Tombak, J-P. Maria, F.T. Ayguavives, Z. Jin, G.T. Stauf, A.I. Kingon, and A. Mortazawi, "Voltage-Controlled RF Filters Employing Thin-Film BariumStrontiumTitanate Tunable Capacitors", *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 2, pp. 462–467, February 2003.

[112] I.B. Vendik, O.G. Vendik, and E.L. Kollberg, "Commutation Quality Factor of Two-state Switchable Devices", *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 5, pp. 802–808, May 2000.

[113] T.H. Lee, *Planar Microwave Engineering*, Cambridge University Press, 2004, pages 233–237.

[114] Z. Ma, A.J. Becker, P. Polakos, H. Huggins, J. Pastalan, H. Wu, K. Watts, Y. H. Wong, and P. Mankiewich, "RF Measurement Technique for Characterizing Thin Dielectric Films", *IEEE Transactions on Electron Devices*, vol. 45, no. 8, pp. 1811–1816, August 1998.

[115] A. Vorobiev, P. Rundqvist, K. Khamchane, and S. Gevorgian, "Silicon Substrate Integrated High Q-factor Parallel-plate Ferroelectric Varactors for Microwave/Millimeterwave Applications", *Applied Physics Letters*, vol. 85, no. 15, pp. 3144–3146, October 2003.

[116] Y. Kim, J. Oh, T-G. Kim, and B. Park, "Effect of Microstructures on the Microwave Dielectric Properties of $ZrTiO_4$ Thin Films", *Applied Physics Letters*, vol. 78, no. 16, pp. 2362–2365, April 2001.

[117] D.C. Dube, J. Baborowski, P. Muralt, and N. Setter, "The Effect of Bottom Electrode on the Performance of Thin Film Based Capacitors in the Gigahertz Region", *Applied Physics Letters*, vol. 74, no. 23, pp. 3546–3548, June 1999.

[118] D.A. Frickey, "Conversions between S, Z, Y, H, $ABCD$, and T Parameters Which are Valid for Complex Source and Load Impedances", *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 2, pp. 205–211, February 1994.

[119] (1983-2009), "The Sonnet website. Online", Available: http://www.sonnetsoftware.com/.

[120] S.B. Cohn, "Problems in Strip Transmission Lines", *IEEE Transactions on Microwave Theory and Techniques*, vol. 3, no. 2, pp. 119–126, March 1955.

[121] P. Rundqvist, A. Vorobiev, S. Gevorgian, and K. Khamchane, "Non-Destructive Microwave Characterization of Ferroelectric Films on Conductive Substrates", *Integrated Ferroelectrics*, vol. 60, no. 1, pp. 1–19, February 2004.

[122] Agilent technologies, "New technologies for accurate impedance measurement (40 Hz to 110 MHz)", Available online: http://www.agilent.com/, 2000, Product Note Agilent PN 4294A.

[123] Agilent Technologies Co. Ltd, "The Impedance Measurement Handbook", Available online: http://www.agilent.com/, July 2006.

[124] P.K. Petrov, N.McN. Alford, and S. Gevorgyan, "Techniques for Microwave Measurements of Ferroelectric Thin Films and Their Associated Error and Limitations", *Measurement Science and Technology*, vol. 16, no. 2, pp. 583–589, January 2005.

[125] (2009), "The Cascade Microtech Website. Online", Available: http://www.cmicro.com/.

[126] C. Wenbin, K.G. McCarthy, and A. Mathewson, "Practical Considerations for Measurements of Test Structures for Dielectric Characterization", *IEEE International Conference on Microelectronic Test Structures*, pp. 221–225, March 2009.

[127] S.A. Wartenberg, *RF Measurements of Die and Packages*, Artech House Publishers, 2002.

[128] (2009), "The Picosecond Website. Online", Available: http://www.picosecond.com/.

[129] M.P.J. Tiggelman, K. Reimann, and J. Schmitz, "Reducing AC Impedance Measurement Errors Caused by the DC Voltage Dependence of Broadband High-voltage Bias-tees", *IEEE International Conference on Microelectronic Test Structures*, pp. 200–205, March 2007.

[130] (1996-2009), "The MatWeb Website. Online", Available: http://www.matweb.com/.

[131] (2003-2008), "The Hoya Corporation USA Optics Division Website. Online", Available: http://www.hoyaoptics.com.

[132] F.A. Miranda, G. Subramanyam, F.W. Van Keuls, R.R. Romanofsky, J.D. Warner, and C.H. Mueller, "Design and Development of Ferroelectric Tunable Microwave Components for Ku- and K-band Satellite Communication Systems", *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 7, pp. 1181, July 2000.

[133] J. Tamaki, G.K.L. Goh, and F.F. Lange, "Novel Epitaxial Growth of Barium Titanate Thin Films by Electrodeposition", *Journal of Materials Research*, December 2000.

[134] D. Ghosh, B. Laughlin, J. Nath, A.I. Kingon, M.B. Steer, and J.-P. Maria, "Tunable High-quality-factor Interdigitated (Ba,Sr)TiO_3 Capacitors Fabricated on Low-cost Substrates with Copper Metallization", *Thin Solid Films*, vol. 496, pp. 669–673, February 2006.

[135] A.C. Reyes, S.M. El-Ghazaly, S.J. Dorn, M. Dydyk, D.K. Schroder, and H. Patterson, "Coplanar Waveguides and Microwave Inductors on Silicon Substrates", *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, no. 9, pp. 2016–2022, May 1995.

[136] J.T.M. van Beek, M.H. W.M. van Delden, A. van Dijken, P. van Eerd, M. van Grootel, A.B.M. Jansman, A.L.A.M. Kemmeren, Th.G.S.M. Rijks, P.G. Steeneken, J. den Toonder, M. Ulenaers, A. den Dekker, P. Lok, N. Pulsford, F. van Straten, L. van Teeffelen, J. de Coster, and R. Puers, "High-Q Integrated RF Passives and Micromechanical Capacitors on Silicon", *Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 3–6, September 2003.

[137] H.N. Al-Shareef, D. Dimos, B.A. Tuttle, and M.V. Raymond, "Metallization Schemes for Dielectric Thin Film Capacitors", *Journal of Materials Research*, vol. 12, no. 2, pp. 347–354, 1997.

[138] J.W. Niemantsverdriet, *Spectroscopy in catalysis*, Wiley-VCH, 2nd edition, 2000, p.86.

[139] J.O. Olowolafe, R.E. Jones, Jr., A.C. Campbell, R.I. Hetide, C.J. Mogab, and R.B. Gregory, "Effects of Anneal Ambients and Pt Thickness on Pt/Ti and Pt/Ti/TiN Interfacial Reactions", *Journal of applied physics*, vol. 73, no. 4, pp. 1764–1772, February 1993.

[140] A. Ehrlich, U. Weiš, W. Hoyer, and T. Geš̈ner, "Microstructural Changes of Pt/Ti Bilayer During Annealing in Different Atmospheres an XRD Study", *Thin Solid Films*, vol. 300, no. 1–2, pp. 122–130, May 1997.

[141] K-B. Kim and C-S. Park, "Application of RF Varactor Using $Ba_xSr_{1-x}TiO_3/TiO_2$/HR-Si Substrate for Reconfigurable Radio", *IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control*, vol. 54, no. 11, pp. 2227–2232, November 2007.

[142] Y. Xu and J.D. Mackenzie, "Ferroelectric Thin Films Prepared by Sol-Gel Processing", *Integrated Ferroelectrics*, vol. 1, pp. 17–42, April 1992.

[143] J.D. Mackenzie and Y. Xu, "Ferroelectric Materials by the Sol-Gel Method", *Journal of Sol-Gel Science and Technology*, vol. 8, no. 1–3, pp. 673–679, February 1997.

[144] J.I. Langford and A.J.C. Wilson, "Scherrer After Sixty Years: A Survey and Some New Results in the Determination of Crystallite Size", *Journal of Applied Crystallography*, vol. 11, no. 2, pp. 102–113, April 1978.

[145] I.P. Koutsaroff, P. Woo, L. McNeil, M. Zelner, A. Kassam, M. Capanu, L. Chmiel, B. McClelland, and A. Cervin-Lawry, "Dielectric Properties of (Ba,Sr)TiO_3 MOD Films Grown on Various Substrates", *IEEE International Symposium on Applications of Ferroelectrics*, pp. 247–250, May-June 2002.

[146] A. Ioachim, H.V. Alexandru, C. Berbecaru, S. Antohe, F. Stanculescu, M.G. Banciu, M.I. Toacsen, L. Nedelcu, D. Ghetu, A. Dutu and G. Stoica, "Dopant Influence on BST Ferroelectric Solid Solutions Family", *Materials Science and Engineering C*, vol. 26, pp. 1156–1161, July 2006.

[147] T.W. Kim, M. Jung, H.J. Kim, T.H. Park, Y.S. Yoon, W.N. Kang, S.S. Yom, and H.K. Na, "Optical and Electrical Properties of Titanium Dioxide Films with a High Magnitude Dielectric Constant Grown on p-Si by Metalorganic Chemical Vapor Deposition at Low Temperature", *Applied Physics Letters*, vol. 64, no. 11, pp. 1407–1409, March 1994.

[148] J. Robertson, "High Dielectric Constant Gate Oxides for Metal Oxide Si Transistors", *Reports on Progress in Physics*, vol. 69, no. 2, pp. 327–396, December 2006.

[149] P.C. Osbond, N.I. Payne, N.M. Shorrocks, R.W. Whatmore, F.W. Ainger, "Dielectric and Microstructural Properties of Barium Strontium Titanate Ceramics Prepared from Citrate Precursors", *International Symposium on Applications of Ferroelectrics*, pp. 348–351, 1986.

[150] S. Stemmer, S.K. Streiffer, N.D. Browning, and A.I. Kingon, "Accommodation of Nonstoichiometry in (100) Fiber-textured $(Ba_xSr_{1-x})Ti_{1+y}O_{3+z}$ Thin Films Grown by Chemical Vapor Deposition", *Applied Physics Letters*, vol. 74, no. 17, pp. 2432–2434, April 1999.

[151] D.E. Kotecki, J.D. Baniecki, H. Shen, R.B. Laibowitz, K.L. Saenger, J.J. Lian, T.M. Shaw, S.D. Athavale, C. Cabral, Jr., P.R. Duncombe, M. Gutsche, G. Kunkel, Y.-J. Park, Y.-Y. Wang, and R. Wise, "(Ba,Sr)TiO_3 Dielectrics for Future Stacked-capacitor DRAM", *IBM Journal of Research and Development*, vol. 43, no. 3, pp. 367–382, May 1999.

[152] T.R. Taylor, P.J. Hansen, B. Acikel, N. Pervez, R.A. York, S.K. Streiffer, and J.S. Speck, "Impact of Thermal Strain on the Dielectric Constant of Sputtered Barium Strontium Titanate Thin Films", *Applied Physics Letters*, vol. 80, no. 11, pp. 1978–1980, March 2002.

[153] (2000-2009), "The Agilent Website. Online", Available: http://www.agilent.com/.

[154] O.G. Vendik and S.P. Zubko, "Modeling the Dielectric Response of Incipient Ferroelectrics", *J.Appl.Phys.*, vol. 82, no. 9, pp. 4475–4483, November 1997.

[155] M.C. Chiu, C.C. Wang, H.C. Yao, and F.S. Shieu, "Microstructure and Electrical Properties of $Ba_{1-x}Sr_xTiO_3$ Thin Films Prepared by RF Magnetron Sputtering", *Materials Chemistry and Physics*, vol. 94, no. 1, pp. 141–147, November 2005.

[156] H.B. Sharma and H.N.K. Sarma, "Electrical Properties of Sol-gel Processed Barium Titanate Films", *Thin Solid Films*, vol. 330, no. 2, pp. 178–182, September 1998.

[157] C. Hutton, *Course of Mathematics*, vol. 2, Gilbert & Rivington, 7^{th} edition, 1837.

[158] J. Nath, D. Ghosh, J-P. Maria, A.I. Kingon, W. Fathelbab, P.D. Franzon, and M.B. Steer, "An Electronically Tunable Microstrip Bandpass Filter Using Thin-Film BariumStrontiumTitanate (BST) Varactors", *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 9, pp. 2707–2712, September 2005.

[159] A. Tombak, "A Ferroelectric-Capacitor-Based Tunable Matching Network for Quad-Band Cellular Power Amplifiers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 2, pp. 370–375, February 2007.

[160] M.K. Roy and J. Richter, "Tunable Ferroelectric Filters for Software Defined Tactical Radio", *IEEE Ultrasonics, Ferroelectrics, and Frequency Control*, vol. , no. , pp. 1–4, 2006.

[161] I.C. Hunter, *Theory and Design of Microwave Filters*, Institution of Engineering and Technology, April 2001.

[162] (2009), "Federal Standard 1037C Website. Telecommunications: Glossary of Telecommunication Terms Online", Available: http://www.its.bldrdoc.gov/fs-1037/fs-1037c.htm/.

[163] G.L. Matthaei, L. Young and E.M.T. Jones, *Microwave Filters, Impedance-Matching Networks and Coupling Structures*, Artech House, 1985.

[164] R. Levy, R.V. Snyder, and G. Matthaei, "Design of Microwave Filters", *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. , March 2002.

[165] J.B. Thomas, "Cross-coupling in Coaxial Cavity Filters - A Tutorial Overview", *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 4, pp. 1368–1376, April 2003.

[166] (2008), "The Coilcraft Website. Online", Available: http://www.coilcraft.com.

[167] W. Middleton and M.E. Van Valkenburg, *Reference Data for Engineers: Radio, Electronics, Computers and Communications*, Newness Press, 9$^{\text{th}}$ edition, 2002.

[168] K.-C. Wan and Q. Xue, "Simple Adaptive Matching Antenna", *Electronics Letters*, vol. 43, no. 14, pp. , July 2007.

[169] M. Okoniewski and M.A. Stuchly, "A Study of the Handset Antenna and Human Body Interaction", *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 10, pp. 1855–1864, October 1996.

[170] T. Huang and K.R. Boyle, "User Interaction Studies on Handset Antennas", *The Second European Conference on Antennas and Propagation (EuCAP)*, vol. , no. , pp. 1–6, November 2007.

[171] C. Hoarau, N. Corrao, J.-D. Arnould, P. Ferrari, and P. Xavier, "Complete Design and Measurement Methodology for a Tunable RF Impedance-Matching Network", *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 11, pp. 2620–2627, November 2008.

[172] J.F. White, *High Frequency Techniques: An Introduction to RF and Microwave Engineering*, Wiley-Interscience, 2004.

[173] Y. Sun and J.K. Fidler, "Design Method for Impedance Matching Networks", *IEEE Proceedings Circuits, Devices and Systems*, vol. 143, no. 4, pp. 186–194, August 1996.

[174] B. Chung, "Q-based Design Method for T-network Impedance Matching", *Microelectronics Journal*, vol. 37, no. 9, pp. 1007–1011, September 2006.

Summary

In this thesis, the results of intensive electrical characterization, modeling and the design of hardware with thin film tunable capacitors, i.e., dielectric varactors, has been presented and discussed. Especially the quality factor Q and the tuning ratio η of the tunable capacitors have been studied, since these are crucial parameters for reconfigurable RF front-end applications for mobile phones.

In Chapter 2, a literature survey was summarized describing the state of the art Q and η for different tunable capacitor technologies based on varactor diodes, dielectric varactors, semiconductor-switched capacitors, and micro-machined electro mechanical systems. The $Q(\eta)$ relations were described separately by using basic physical models. However, the relations could be described with a single $Q(\eta)$ formula. The study concludes that RF micro-electro-mechanical switches have the highest tuning potential with a high Q, but are relatively large in size. For continuous, moderate tuning ranges highly doped GaAs varactor diodes could offer the best performance. Dielectric varactors will be most attractive for small physical size and low cost devices.

In Chapter 4, it was discussed how RF tunable capacitors based on thin film barium strontium titanate (BST) were designed, fabricated, and measured. In addition, a dedicated analysis technique was developed to separate the electrical dissipation in the resistive electrodes from the dissipation in the dielectric oxide films.

In Chapter 5 it was shown how voltage-dependent impedance measurement errors, using a commercial wide-band bias-tee, could be prevented in RF $C(V_{\mathrm{dc}})$ measurements by an additional open calibration or by employing a custom-made wide-band bias-tee.

In Chapter 6, the Q and η were studied as a function of barium to strontium composition and doping in the BST films. A higher Q and a lower η was measured for a lower barium content in the BST films. Cation doping in the BST films can have a similar effect. The electrical characterization results were utilized as an input to further improve the capacitors RF performance.

In Chapter 7, a ferroelectric capacitor model has been implemented as a new component in the design environment ADS. The model can describe a $C(V_{\mathrm{dc}})$ measurement by incorporating only 4 fit parameters.

In Chapter 8, a 2^{nd} order bandpass transmit filter and a low-pass impedance matching network was designed and simulated in ADS, to obtain the $Q(\eta)$ requirements for ferroelectric capacitors. A very high Q was required in the filter for the inductor and capacitor components to fulfill the customer specifications. Furthermore, an adaptive antenna impedance matching network was designed and simulated for a user, which covers the antenna with his hand resulting in a de-tuned antenna. Two cascaded low-pass L-sections improved the antenna impedance matching. The simulation results, using practical feasible values for the components, for the latter networks pointed out that tunable ferroelectric capacitors are promising components.

Summarizing this thesis, the simulations and device characterization provided the link between the applications and the performance requirements of tunable capacitors. This could be the basis to optimize the ferroelectric materials and devices for RF applications.

Samenvatting

In dit proefschrift zijn de resultaten gepresenteerd en besproken die verkregen zijn door middel van intensieve elektrische karakterisatie van teststructuren, diverse simulaties en hardware ontwerpen gebaseerd op elektrisch regelbare capaciteiten met een dunne diëlektrische laag (zogenaamde diëlektrische varicaps). Met het oog op de integratie van deze componenten in RF front-end toepassingen, lag de nadruk op het bestuderen van de kwaliteitsfactor Q en de ratio η die aangeeft in welke mate de capaciteit elektrisch geregeld kan worden.

In Hoofdstuk 2 is een literatuuroverzicht samengevat van de beste gepubliceerde data voor de Q en η van verschillende elektrisch regelbare capaciteiten, waaronder varicap diodes, diëlektrische varicaps, halfgeleidergeschakelde capaciteiten en micro-elektromechanische systemen (MEMS). De $Q(\eta)$ relaties zijn los van elkaar beschreven door gebruik te maken van eenvoudige fysische modellen. Desalniettemin, kunnen de relaties beschreven worden met een enkele $Q(\eta)$ vergelijking. Het resultaat van de studie laat zien dat RF-MEMS schakelaars de hoogst mogelijke η kunnen krijgen samen met een hoge Q, maar dat deze structuren relatief grote afmetingen hebben. Voor continue elektrisch regelbare capaciteiten met een middelmatige η geven hoog gedoteerde GaAs varactor diodes de beste prestaties. Diëlektrische varicaps zijn het meest aantrekkelijk als kleine dimensies en lage kosten voor de capaciteit van belang zijn.

In Hoofdstuk 4 is gediscussieerd hoe de diëlektrische varicaps, gebaseerd op barium strontium titanaat (BST), ontworpen, gefabriceerd en gemeten zijn. Ook is er een speciale analysetechniek ontwikkeld die de elektrische dissipatie veroorzaakt door de niet-ideale elektroden en door de diëlektrische laag van elkaar kan scheiden.

In Hoofdstuk 5 is aangetoond dat spannings-afhankelijke meetfouten kunnen ontstaan bij impedantie metingen, indien een commerciële breedbandige bias-tee wordt gebruikt. Twee oplossingen worden aangedragen om deze meetfouten te voorkomen door middel van een extra open calibratie of door gebruik te maken van een zelf ontwikkelde breedbandige bias-tee.

In Hoofdstuk 6 zijn de Q en de η bestudeerd als functie van de hoeveelheid barium en doping in dunne BST lagen. Een hogere Q en een lagere η zijn gemeten bij een lagere hoeveelheid barium in de BST films. Een kation

doping in de BST films kan hetzelfde effect hebben. De resultaten van de elektrische karakterisatie droegen bij om inzicht te krijgen hoe de RF prestaties van de diëlektrische varicaps verder verbeterd konden worden.

In Hoofdstuk 7 is besproken hoe een model van een diëlektrische varicap geïmplementeerd is als een nieuw electronisch component in een circuit ontwerpprogramma, genaamd ADS. Het model is in staat om het gedrag te beschrijven van een gemeten capaciteits-spannings meting door gebruik te maken van enkel 4 parameters in het model.

In Hoofdstuk 8 is het ontwerp besproken van een 2^{e} orde banddoorlaatfilter dat gesimuleerd is in ADS om de eisen te achterhalen waaraan de elektrisch regelbare capaciteiten aan moeten voldoen met betrekking tot de Q en de η. Een hele hoge Q was vereist voor de gebruikte spoelen en capaciteiten om te voldoen aan de eisen van de klant. Daarnaast is een regelbaar impedantie "matching" netwerk voor een antenne ontworpen en gesimuleerd voor een antenna waarvan de impedantie verandert. Twee laagdoorlaatfilters in een L-vorm zijn aan elkaar geschakeld om de antenne impedantie "matching" te verbeteren. De simulatieresultaten, die tot stand zijn gekomen met realistische componentwaarden, van de laatst genoemde netwerken laten zien dat diëlektrische varicaps veelbelovende componenten zijn om te gebruiken.

Dit proefschrift laat door middel van simulaties en teststructuur karakterisatie, de link zien tussen de RF toepassingen en de $Q(\eta)$ prestaties waaraan een diëlektrische varicap moet voldoen. Dit kan de basis zijn om de ferroelektrische materialen en de componenten (bouwstenen) verder te verfijnen voor het gebruik in toepassingen.

List of publications

Filed EU patents

- Y. Furukawa, K. Reimann, F. Jedema, **M.P.J. Tiggelman**, and A. Roest, Application number 81340402EP01, May 2008.
- **M.P.J. Tiggelman** and K. Reimann, Application number 81049445EP01, August 2008.

Journal publications

- M. Klee, H. Van Esch, W. Keur, B. Kumar, L. van Leuken-Peters, J. Liu, R. Mauczok, K. Neumann, K. Reimann, Ch. Renders, A.L. Roest, **M.P.J. Tiggelman**, M. De Wild, O. Wunnicke, and J. Zhao, *Ferroelectric Thin-Film Capacitors and Piezoelectric Switches for Mobile Communication Applications*, IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, vol. 56, no. 8, pp. 1505–1512, August 2009.
- **M.P.J. Tiggelman**, K. Reimann, F. Van Rijs, J. Schmitz, and R.J.E. Hueting, *On the Trade-Off Between Quality Factor and Tuning Ratio in Tunable High-Frequency Capacitors*, IEEE Transactions on Electron Devices, vol. 56, no. 9, pp. 2128-2136, September 2009.
- **M.P.J. Tiggelman**, K. Reimann, M. Klee, R. Mauczock, W. Keur, and R.J.E. Hueting, $Ba_xSr_{1-x}Ti_{1.02}O_3$ *Metal-Insulator-Metal Capacitors on Planarized Alumina Substrates*, Thin Solid Films (2009), doi:10.1016/j.tsf.2009.09.049

Conference proceedings

- M. Klee, D. Beelen, W. Keur, R. Kiewitt, B. Kumar, R. Mauczok, K. Reimann, Ch. Renders, A. Roest, F. Roozeboom, P.G. Steeneken, **M.P.J. Tiggelman**, F. Vanhelmont, O. Wunnicke, P. Lok, K. Neumann, J. Fraser, and G. Schmitz, *Application of Dielectric, Ferroelectric and Piezoelectric Thin Film Devices in Mobile Communication and Medical Systems*, IEEE International Symposium on the Applications of Ferroelectrics (ISAF), pp. 9–16, July 2006.

- **M.P.J. Tiggelman**, K. Reimann, M. Klee, D. Beelen, W. Keur, J. Schmitz, and R.J.E. Hueting, *Electrical Characterization of Thin Film Ferroelectric Capacitors*, Proceedings of the workshop on Semiconductor Advances for Future Electronics and Sensors (SAFE), pp. 439–443, November 2006.
- **M.P.J. Tiggelman**, K. Reimann, and J. Schmitz, *Reducing AC Impedance Measurement Errors Caused by the DC Voltage Dependence of Broadband High-voltage Bias-tees*, Proceedings of the ICMTS conference, pp. 200–205, March 2007.
- **M.P.J. Tiggelman**, K. Reimann, M. Klee, J. Schmitz, R.J.E. Hueting, J. Liu, Y. Furukawa, R. Mauczock, and W. Keur, *Separation of Intrinsic Dielectric and Resistive Electrode Losses in Ferroelectric Capacitors at Radio Frequencies*, Proceedings of the SAFE conference, pp. 465–467, November 2007.
- M. Klee, W. Keur, R. Mauczok, H. van Esch, M. de Wild, J. Liu, A. Roest, K. Reimann, Ch. Renders, L. Peters, **M.P.J. Tiggelman**, O. Wunnicke, and K. Neumann, *MI004 Miniaturised, High Performance Ferroelectric and Piezoelectric Thin Film Devices*, ISAF, pp. 1–4, February 2008.
- **M.P.J. Tiggelman**, K. Reimann, J. Liu, M. Klee, W. Keur, R. Mauczock, J. Schmitz, and R.J.E. Hueting, *Identifying Dielectric and Resistive Electrode Losses in High-density Capacitors at Radio Frequencies*, Proceedings of the ICMTS conference, pp. 190–195, March 2008 (***oral presentation***).
- **M.P.J. Tiggelman**, K. Reimann, J. Liu, M. Klee, R. Mauczok, W. Keur, J. Schmitz, and R.J.E. Hueting, *The Trade-off Between Tuning Ratio and Quality Factor of* $Ba_xSr_{1-x}TiO_3$ *MIM Capacitors on Alumina Substrates*, Proceedings of the SAFE conference, pp. 506–508, November 2008.
- M. Klee, H. Boots, B. Kumar, Ch. Van Heesch, R. Mauczok, W. Keur, M. de Wild, H. Van Esch, A. Roest, K. Reimann, L. van Leuken, O. Wunnicke, G. Schmitz, M. Mienkina, M. Mleczko, and **M.P.J. Tiggelman**, *Ferroelectric and Piezoelectric Thin Films and their Applications for Integrated Capacitors and Piezoelectric Ultrasound Transducers*, European Materials Research Society 2009, Accepted for publication.

- R.W. Herfst, P.G. Steeneken, **M.P.J. Tiggelman**, J. Stulemeijer, and J. Schmitz, *Fast RF-CV Characterization Through High-Speed 1-port S-parameter Measurements*, ICMTS conference 2010, Abstract accepted.

Dankwoord

Vooruitkijkend op het behalen van mijn opleiding elektrotechniek destijds aan de Universiteit Twente (UT) vroeg mijn zus: “What’s next, doc?”. Ook Jurriaan stelde mij deze vraag (in andere bewoordingen). Hij gaf aan dat hij een leuke en uitdagende promotieopdracht had openstaan bij Philips Research in Eindhoven. Na verschillende goede gesprekken met diverse mensen, waaronder Jurriaan Schmitz, Rob Wolters, Radko Bankras, Mareike Klee, Klaus Reimann en Ronald Wolf sloeg de spreekwoordelijke vonk meerdere malen over en heb ik besloten deze opdracht met beide handen aan te grijpen.

In 2005 ben ik vol met goede moed gestart aan mijn promotieonderzoek. Mijn laatste 4 levensjaren heb ik kennisgemaakt met een hoop collegae bij de UT, Philips Research en NXP Semiconductors met wie ik minstens *één* passie deel namelijk de passie voor de techniek. Het resultaat van een hoop metingen, simulaties en goede gesprekken heeft uiteindelijk geleid tot het resultaat op uw tafel.
Een deel van mijn resultaten zijn mogelijk gemaakt door het NANOSTAR project waar NXP deel van uitmaakte. Bij deze wil ik de Europese commissie bedanken voor de financiële ondersteuning van dit project.

Mijn promotor, Jurriaan Schmitz, zou ik graag bedanken voor de mogelijkheid die hij mij heeft gegeven om dit promotieonderzoek te mogen voltooien, het meedenken met het geven van richting aan mijn onderzoek, het zien van kansen om artikelen te schrijven en het doen toekomen van zijn kritische kijk op geschreven teksten. Ook Ray Hueting, als assistent-promotor, wil ik nadrukkelijk bedanken. Ray, bedankt voor jouw altijd enthousiaste betrokkenheid, nauwgezette en snelle terugkoppeling op geschreven teksten en het laagdrempelige contact.
Ondanks dat ik in Eindhoven mijn onderzoek deed heb ik goede herinneringen overgehouden aan het contact met de vakgroep en mensen van vloer 3 in binnen-en buitenland. Ik kijk met veel plezier terug op de gezellige vakgroepuitjes, borrels en de altijd warme ontvangst bij (voor sommigen) spontane bezoekjes aan de vakgroep. De eerste plezierige herinneringen die bij mij opkomen zijn: het spontaan creëren van een flexplek in het kantoor van Ihor, ontvangst met geïmporteerde vers gezette espresso van Giulia of koffie door Annemiek en de gesprekken in de gang met Arjen en Bijoy. Op andere plekken heb ik de mensen van “vloer 3” ook beter leren kennen.

Om maar een voorbeeld te noemen: een avond na een conferentie zaten we (ik zal geen namen noemen) in een karaoke bar met een microfoon in de ene hand (ongegeneerd hard meezingend in een afgesloten ruimte) en een geel drankje, met silicium als bestandsdeel, in de andere hand. Voorts wil ik graag alle mensen van vloer 3 bedanken voor het creëren van een fijne werksfeer gedurende de laatste jaren.

De laatste jaren heb ik 3 groepsleiders gehad, die het allen voor mij mogelijk maakten om mijn onderzoek voor te zetten. Ronald Wolf, Derk Reefman en Reinout Woltjer bedankt voor onze prettige samenwerking. In mijn multidisciplinaire projectgroep beschouw ik het als een voorrecht om te hebben mogen werken met Mareike Klee, Klaus Reimann, Aarnoud Roest, Daniëlle Beelen, Ruediger Mauczock, Wilco Keur, Jin Liu en Yukiko Furikawa. In mijn ogen hebben wij in teamverband laten zien dat de "kwaliteitsfactor" dusdanig van aard was, dat deze heeft geleid tot mooie onderzoeksresultaten en het succesvol afronden van het EU project. Naast de hiervoorgenoemde collegae wil ik uitdrukkelijk Mareike en Klaus bedanken voor hun vertrouwen in mij, de leerzame, stimulerende en de fijne persoonlijke gesprekken, de plezierige samenwerking en het vergroten van mijn capaciteit met betrekking tot het begrip van ferroelektrische materialen en hun gedrag. Aarnoud, aan jou wil ik ook mijn dank betuigen als projectleider, als collega, als goede gesprekspartner en als fervent tennisspeler!
Mijn kamergenoten Jos, Loic, Rienk, Olaf en Krishnan wil ik zeker niet onderbelichten. Het werken, lunchen en koffie drinken in jullie aanwezigheid maakte mijn werkdag net weer iets aangenamer en completer. Het leeuwendeel van de tijd op de werkplek heb ik doorgebracht met Olaf, die ik wil bedanken voor onze interessante discussies over taal, techniek, voertuigen, Twente ("ligt dat in Friesland?") en reizen. Voorts heb ik met de overige collegae ook nuttige en leerzame gesprekken gevoerd, waaronder met Friso, Peter S., Frederick, Martijn, Deepu ("thanks for being such a good friend and for being my paranymph"), Hans, Pietro, Martijn, André, Fred, John S., Jeroen, Ralf, Kim, Twan, Geert, Stefan, Anja, Vicki, Isabella, John M., Johan, Harry, Christel, Marco, Biju en Peter D. De materiaal analyse groep van Philips verdient ook zeker een pluim en wil ik bij deze bedanken voor hun bijdrage in het onderzoeken van de test structuren. Ik wil Martijn Goossens bedanken voor het geven van een introductie en het gebruik van specialistische meetapparatuur. Ralf Pijper wil ik bedanken voor het doen van RF metingen met zijn meetopstelling en Anton De Graauw voor de

leerzame gesprekken over “impedance matching networks” en het kritisch doornemen van een van mijn artikelen ten behoeve van een publicatie. Dit laatste geldt zeker ook voor Klaus, Mareike, Aarnoud, Olaf, Hans Tuinhout, John Mills en Leon Vogels. Jullie inbreng heeft mij veel inzicht gegeven in hoe je een duidelijke publicatie schrijft waarin ook het bedrijf zich kan vinden, bedankt! Ook buiten werktijd heb ik veel plezier beleefd met collegae o.a. tijdens sectoruitjes, het vieren van carnaval in vol ornaat (ik zal geen namen noemen), het tennissen of het maken van een fietstocht, tijdens diners en het drinken van een speciaal biertje zo nu en dan.

Ook de promotiecommissie wil ik nadrukkelijk bedanken voor het nemen van de moeite om mijn proefschrift door te nemen en om met mij van gedachten te wisselen en mij te woord te staan tijdens de verdediging.

Aan het studeren heb ik in de loop der jaren vrienden en vriendinnen overgehouden, die ik hierbij ook wil bedanken voor alle memorabele en motiverende momenten die ik met hun (en hun lieftallige partners) heb beleefd: Bart, Wesley, Jurgen, Maurice, Jeroen, Jeroen L., Dennis en Nancy, Jaap, Ard, Tonnie en Michael, Marcus, Alex, Gerbert, Arno, Frank, René en Eric.

Pa, Ma, Esther, Gerwen, Tatiana, Ida, opa’s, oma’s en overige familie wil ik in het bijzonder ook bedanken voor hun onvoorwaardelijke steun gedurende mijn jaren als promovendus. Tot slot zou ik mijn verloofde Natalie willen bedanken voor haar steun en toeverlaat. Zelfs tijdens de verdediging zit je aan mijn zijde als paranimf.

Ik kan u verzekeren dat deze gehele periode in vele opzichten in zakelijke- maar zeker ook in persoonlijke sfeer zeer intensief is geweest, waarbij ik heel veel te danken heb gehad aan vele mensen. Het is dan ook onvermijdelijk dat ik wellicht iemand heb vergeten te vernoemen. Indien jij ook een steentje hebt bijgedragen aan het welslagen van mijn promotieonderzoek en de behaalde resultaten, wil ik je vanaf deze plaats nadrukkelijk bedanken.

Tenslotte, een Tiggel is een baksteen. Als Tiggel-man heb ik op professioneel niveau de laatste 4 jaar zeer intensief gewerkt aan een bouwsteentje op microniveau. In parallel met mijn onderzoek heb ik op het persoonlijke niveau samen met Natalie onze macro-relatie verder verstevigd. Onze liefde is bekroond met de geboorte van onze eigen D.*r.* Tiggelman. Wat een geluk die initialen en wat een genot die zoon!

In 2009 komt het leven als (“Ph.D.”) student aan zijn einde. Er is nooit een laatst einde, er is altijd weer een nieuw begin.

Biography

Markus Petrus Josephus Tiggelman was born on the 4th October 1977 in Enschede, the Netherlands. After finishing his pre-university education level ("VWO") in 1998 he continued his education at the Saxion higher technical school (HTS) in Enschede, where he received his B.Sc. degree in Electrical Engineering with his major in Telecommunication in 2002. Afterwards, he decided to obtain a more solid theoretical background in electrical engineering. For this reason, he started his master study at the University of Twente (UT) in Enschede at the department of Electrical Engineering, Mathematics and Computer Science with his major in microsystems and microelectronics. He obtained his M.Sc. degree from the UT in 2005. During his master assignment at the chair of semiconductor components, he designed and electrically characterized low resistance teststructures for gate dielectrics with a high leakage current. At the same chair, he started his Ph.D. research in October 2005 and was fulltime detached at Philips Research Laboratories and later at NXP Semiconductors in Eindhoven, the Netherlands. In November 2009, he completed his dissertation entitled "Thin Film Barium Strontium Titanate Capacitors for Tunable RF Front-end Applications".